University of Alberta

Pulsed Current Electrodeposition of Sn and Sn-Cu Films

by

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Dedication

To my son Aidan: Your arrival was a very welcome distraction from this work.

Abstract

This work considers electrodeposited Sn-Cu films for electronic packaging using an additive-free sulphate bath. A background of packaging techniques is given, and eutectic Sn-Cu is set within this context. The films were deposited onto Au- and Cu-coated Si wafers, and wrought Cu. Morphology, coverage and composition are surveyed under a variable set of direct- and pulsed-current parameters. It is determined that pulse duty and average current density have a marked effect on the films. Solderability trials produced well-covered films on wrought Cu substrates. Citric acid additions were studied for use as a bath stabilizer.

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List of Symbols

$(\partial N/\partial t)(1/A)$ = deposition rate from the source with area A
α = coefficient of evaporation (higher with cleaner source surface)
= transfer coefficient, which is a measure of oxidation vs. reduction barrier symmetry
δ = boundary layer thickness
δ_p = diffusion layer thickness
ε = required double layer charging potential in volts
κ = specific conductivity
η = overpotential
η_s = surface potential
η_k = crystallization potential
ν = nucleation rate
A = area
A_{meas} is the measured plating area
A_{max} is the largest measured plating area
a = activity
C = concentration
C_d = capacitance of the electric double layer
C_{ad}^{∞} = Bulk concentration of adatoms
C_s = saturation concentration
C_{ad} = Adatom concentration at the nucleus
C_∞ = concentration of ions in the bulk of the solution
C_0 is the concentration of ions at the cathode (where x=0)
c_{norm} is the normalized coverage (in percent)
c_{raw} is the actual coverage value determined by EDX analysis
E = the adjusted reduction potential
E^0 = the standard reduction potential (all species at 1M and 298 K)
F is Faraday's constant: 96485.3 C
i = current
j = current density
j_f = faradic current density
j_n = nonfaradic current density
i_{lim} = limiting current
j_{lim} = limiting current density
j_{pk} = peak current density
j_{avg} = average current density
j_P = pulsed current
j_t = total current
j_C = capacitive current (which charges the double layer)
j_F = faradic current (which powers the redox reactions)
j_0 = exchange current density
k = Boltzmann's constant
k_1 = a constant

k_2 = a constant, proportional to the energy required for 2D nucleation
L = characteristic length
m = molecular weight of a substance being evaporated
n is the number of electrons transferred in the redox reaction
p = the pulse duty (specified in percent)
 = hydrostatic pressure on the surface of the source
p" = vapour pressure at evaporant surface
R = gas constant: 8.31447 J/(mol*K)
 = resistance
R_s = resistance of the solution, or plating bath
R_p = polarization resistance at the cathode
$R_{p'}$ = polarization resistance at the anode
T = temperature
t = time
t_{on} is the time at $j = j_{pk}$
t_{off} is the time at $j = 0$
Wa = Wagner number
x = distance from electrode surface

List of Abbreviations

µ-BGA	Micro-Ball Grid Array
AC	Alternating Current
AMD	Advanced Micro Devices
BGA	Ball Grid Array
C4	Controlled Collapse Chip Connection
C4NP	Controlled Collapse Chip Connection, New Process
COB	Chip-On-Board
CPU	Central Processing Unit
CSP	Chip Scale Package
CVD	Chemical Vapour Deposition
DC	Direct Current
DCA	Direct Chip Attach
DIP	Dual Inline Package
DVD	Digital Video Disc
EDX	Energy-Dispersive X-Ray Analysis
EEE	Electric and Electronic Equipment
EPA	Environmental Protection Agency
EPA DfE	Environmental Protection Agency – Design for Environment
EU	European Union
FCIP	Flip Chip-In-Package
FCOB	Flip Chip-On-Board
FIB	Focused Ion Beam
HAL	Hot Air Leveling
HASL	Hot Air Solder Leveling
HER	Hydrogen Evolution Reaction
IBM	International Business Machines
IC	Integrated Circuit
IHP	Inner Helmholtz Plane
IMC	Intermetallic Compound
iNEMI	International Electronics Manufacturing Initiative
I/O	Input/Output
MCM	Multi-Component Module
MEMS	Micro Electro-Mechanical Systems
MSA	Methanesulfonic acid
NHE	Normal Hydrogen Electrode
OHP	Outer Helmholtz Plane
Ompack	Over-Molded Package
OSP	Organic Surface Perservative
PBB	Polybrominated Biphenyl
PBE	Polybrominated diphenyl ether
PBGA	Plastic Ball Grid Array
PC	Pulsed Current
PCB	Printed Circuit Board

PEG	Polyethylene Glycol
PGA	Pin Grid Array
PR	Pulse Reverse
PTFE	Poly Tetra Fluoroethylene
PTH	Plated Through-Hole
PVD	Physical Vapour Deposition
PWB	Printed Wiring Board
QFP	Quad Flat Pack
RAM	Random Access Memory
RDRAM	Rambus Dynamic Random Access Memory
RoHS	Reduction of Hazardous Substances
RMA	Rosin Mildly Activated
RPM	Rotations Per Minute
SAC	Sn-Ag-Cu
SEM	Scanning Electron Microscopy
SiP	System-in-Package
SoC	System-On-Chip
SOJ	Small Outline "J"
SMT	Surface Mount Technology
TAB	Tape Automated Bonding
TCE	Thermal Coefficient of Expansion
TH	Through-Hole
UBM	Under Bump Metallurgy
US	United States
VP	Vice President
WB	Wire Bonding
WEEE	Waste Electric and Electronic Equipment
XRD	X-Ray Diffraction

Chapter 1: Electronic Packaging Methods

Unless otherwise stated, this chapter is a summary of work presented by [Lau & Mayer 1990], [Gilleo 2002], [Blackwell 2000], [Lasky & Morovan 2002] and [Harper 2005].

Introduction

Packaging Concepts

An electronic package is an enabling product that satisfies a number of design requirements. To begin, integrated circuits (or IC's) are fragile devices that must be manufactured in clean rooms, but are used in far less hospitable environments. Therefore, an important driver for electronic packaging is protection from the elements. In addition, IC's are not really useful by themselves; they must somehow be connected to other components such as input/output (I/O) devices and power supplies. To this end, a package serves to *functionalize* an IC through interconnection. During operation, IC's heat up and will tend to expand at different rates than the circuit boards to which they are mounted. This causes a buildup of heat and stress that must also be accommodated by the packaging. Finally, IC packages can aid performance through enhanced cooling. In all cases, these functions must be carried out in a cost-effective manner using inexpensive materials and high production rates.

There are many different types of packages in use today. Figure 1-1 illustrates some important features of a dual inline package (DIP). It is an older design, but the DIP is possibly the most well-known package style. Important components include the substrate (also called a carrier or interposer), a leadframe, and a cover. The substrate is a flat surface to which an IC is bonded that may also contain circuit traces throughout its thickness. If the substrate is plastic, the IC is normally glued to its surface. If it is ceramic, the IC can be bonded by creating an eutectic Au-Si joint whose melting point is lower than pure Si. The leadframe is integrated with the substrate and wrapped downwards around the sides. The

bonding site on each lead is typically plated metal, such as Au. The job of each lead is to conduct electrical signals, power and sometimes even heat to and from the IC. In most cases, the cover is typically made from liquid-cured epoxy, although polymer, ceramic and steel lids are also used on a substrate with walls. The cover can also be integrated with a heat spreader and/or heat sink in order to maximize cooling.

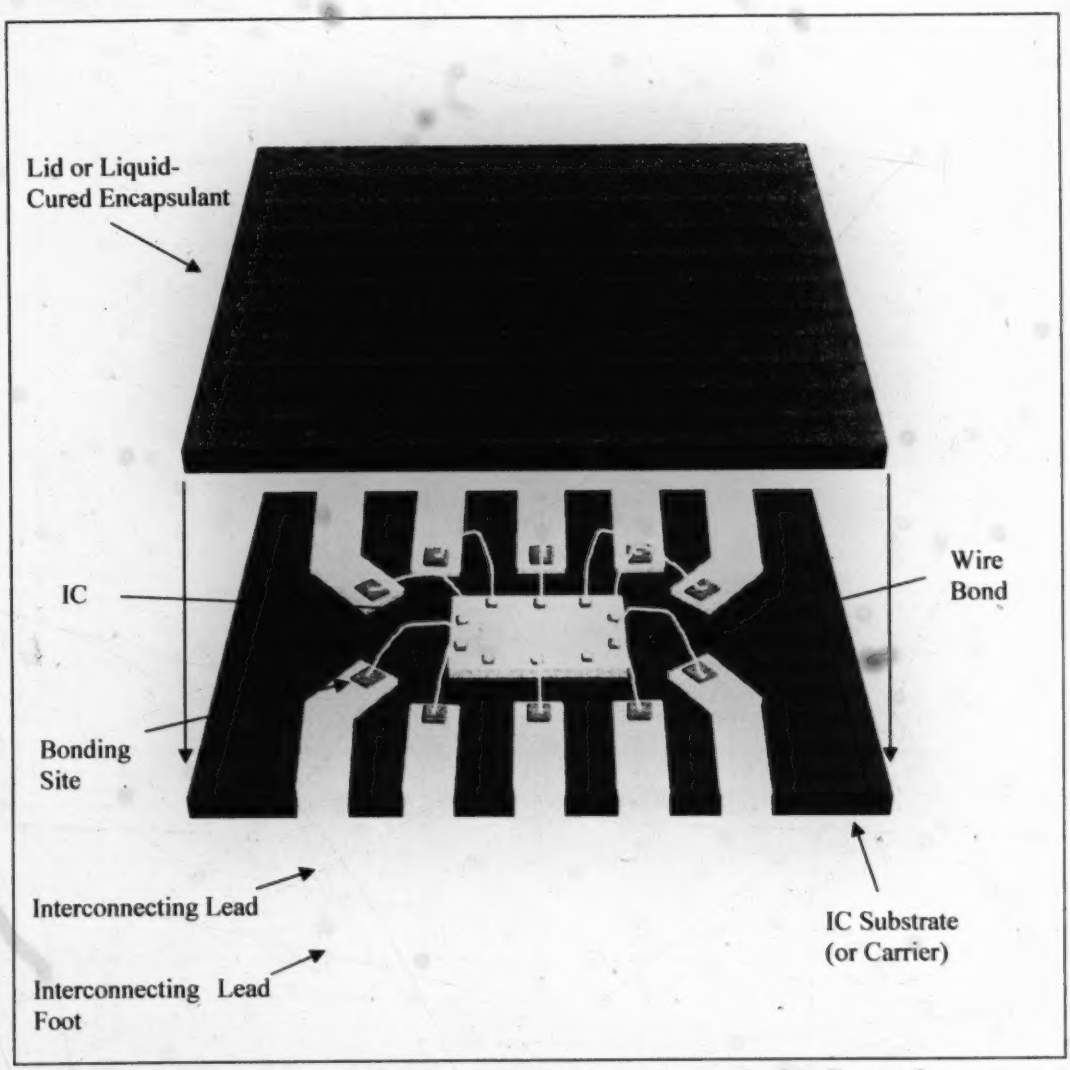

Figure 1-1 – Cross-section of a wire-bonded chip mounted on a dual-in-line package, or DIP. This drawing is based on Figure 15.9 of Mayer and Lau 1990.

Note that the leads on either end of the DIP must be made longer in order to reach the IC. This is a limiting feature of the design, since excessive lead length will degrade performance. Overall, DIPs offer a small number of leads, and therefore a small I/O count. This topic of interconnect density will be discussed later in more detail.

The process of connecting an IC to a substrate is referred to as Level I packaging. When the substrate is connected to a printed wiring board (PWB), this is called Level II packaging. Higher levels of packaging exist, although they are not the subject of this chapter. While several packaging designs are covered in this thesis, extensive reviews are given by [Baldwin & Higgins 2005] and [Manko 1986].

Integrated Circuits and Printed Wiring Boards

Probably the most popular phenomenon in electronics is Moore's Law, which predicts the doubling of IC transistor density every 18 months or so. And while it is impressive, this is really only part of the story, since IC's must ultimately be interconnected with other devices to function.

Figure 1-2 is a section of a computer motherboard. This kind of setup represents a fairly standard interconnection approach for electronic devices, and one could expect similar arrangements of encapsulated IC's on a PWB (also called a PCB, or printed circuit board) inside many other products such as stereos or DVD players. For smaller devices such as cell phones, the on-board packaging density can be a lot higher. High-density packing will be examined in the next chapter.

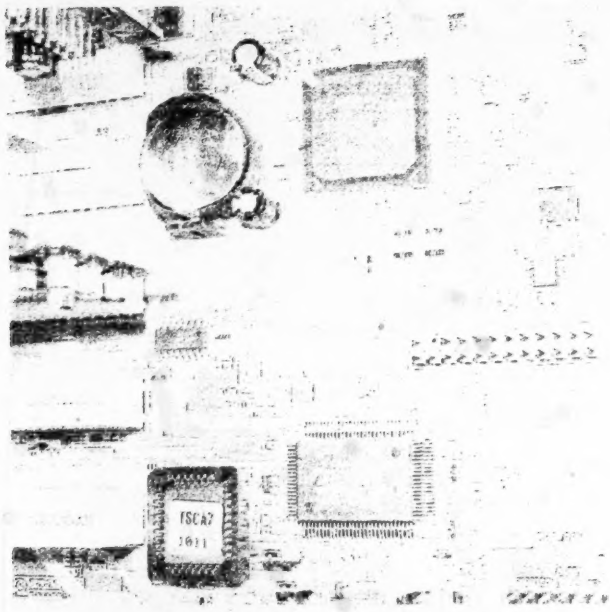

Figure 1-2 – A green-yellow Printed Wiring Board (PWB) that is used to allow IC's (encased in black) to function as a group. Photo by Olsen.

Moore's Law is one half of a coin whose face is constantly shrinking. The smallest features on the Pentium® 4 IC are now 90nm, and may be 65nm by the end of 2005.[1] PWB's represent the other side of the coin, where feature size is not shrinking as quickly. In fact, motherboards have circuit trace widths that are hundreds of micrometers or more. This leaves a thousand-fold difference in scale, and it is the job of an electronic package to bridge the gap.

Naturally, one might consider the assortment of black IC packages in Figure 1-2 and wonder if they could all be integrated on a single chip. For example, consider a CPU IC that contained all of the RAM it required. This sort of idea is being implemented in a number of ways. It is known as System-on-Chip (SoC), but there are obstacles [Khare 2000]. Designs tend to be overly complex, and it is more difficult to customize a single IC design within ever-decreasing product life cycles [Kahn 2004]. Packaging technologies that approach the SoC ideal are multicomponent modules (MCM) and System-In-Package (SiP).

[1] e.g., see www.tomshardware.com

As the IC operates, it will heat up due to electrical resistance effects. Thermal dissipation is a problem that becomes worse with higher levels of circuit integration. As heat is produced, it flows from the IC to the package and finally to the board. A problem is that each component will expand at different rates. Whenever possible, it is desirable to use connections that can reversibly (elastically) deform in response to stress. These are called compliant, and they include the "spider leg" interconnecting leads of a DIP. As will be seen later, there are tradeoffs to consider when using compliant versus noncompliant connections.

To summarize, IC's are packaged in order to fulfill a number of roles. They are made useful through interconnection with other devices. The package helps an IC to *remain* useful by protecting it from the elements, by enhancing heat transfer, and, as will be seen later, by limiting stresses due to thermal expansion mismatch. In this thesis there are two levels of interest: Level I, wherein an IC is attached to a substrate and protected with a cover; and Level II, wherein a Level I package is connected to a PWB. In all cases, a wide level of integration can be achieved, depending on the needs of a device.

Level I (Die to Substrate) Techniques

Wire Bonding (WB)

Wire bonding is an older technology that is well established in the industry. In a straightforward design an IC is bonded face-up on a substrate. Bonding pads on the IC are connected to leads on the substrate using gold or aluminum wire. Figure 1-1 shows a chip (or die) in the center of the substrate that is mounted face-up and gold wire-bonded to the leadframe.

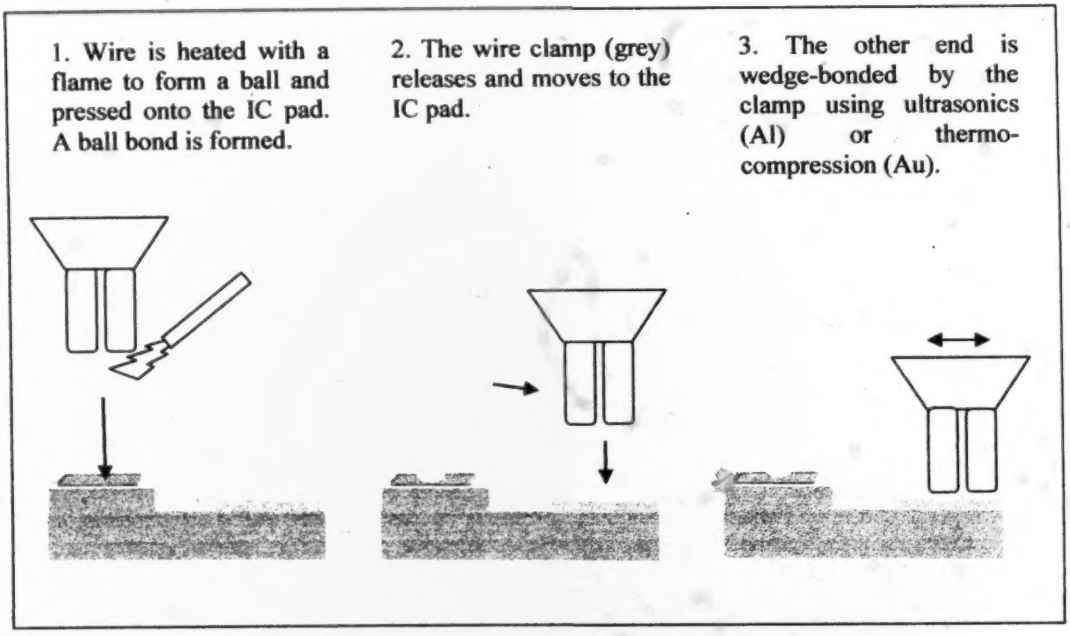
1. Wire is heated with a flame to form a ball and pressed onto the IC pad. A ball bond is formed.
2. The wire clamp (grey) releases and moves to the IC pad.
3. The other end is wedge-bonded by the clamp using ultrasonics (Al) or thermo-compression (Au).

Figure 1-3 - Method of thermal compression bonding. As the name implies, heat and pressure are used to form both the ball and wedge bonds. An important feature is the bonding pads (red). The drawing is based on Fig 1.6 of Gilleo, 2002 and Fig 15.5 from Mayer and Lau 1990.

The wires are joined using a number of techniques, although two distinct types of bonds are formed. The first is called a ball-bond (Step 1 of Figure 1-3), and the second is a wedge bond (Step 3 of Figure 1-3). Wires can start with either type of bond and also end with either type of bond, depending upon the design.

According to the IPC-CM-770 standard (as referenced by Blackwell 2000), Au wire is bonded using either thermocompression or thermosonic methods. Thermosonics uses heat and ultrasonic vibrations to form a metallurgical bond between the wire and the bonding pad. Al wire is bonded to pads using ultrasonics or pure vibrations.

The IPC-CM-770 standard also lists the range of dimensions taken up by wire bonding. This is important, since it sets a limit as to how many wires (or interconnects) can be used, the minimum conduction path between IC and carrier, and finally how much larger the package must be than the IC itself. Figure 1-4

lists these dimensions for thermocompression bonded Au wire, which can accommodate the smallest features.

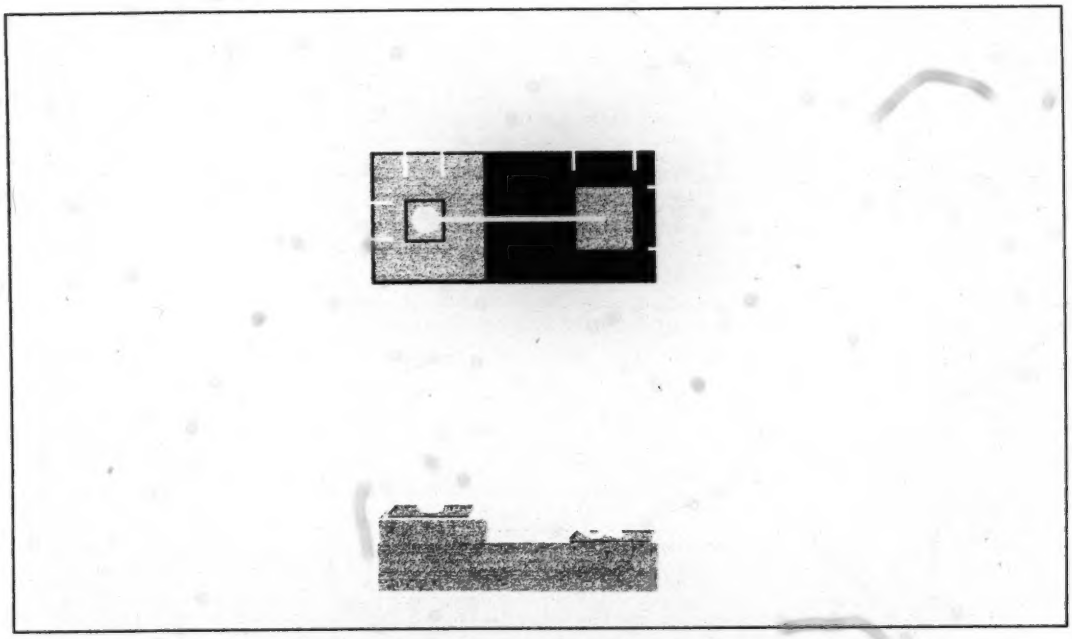

Figure 1-4 - Dimensions for wire bonding, shown from a cutout section of a chip mounted on a carrier. Note that the carrier pad may simply be a coating on a lead. Drawing is based on Fig 4.2 of Blackwell, 2000.

As will be seen, other Level I methods (such as flip chip and chip-scale packaging) are slowly taking over from wire bonding. However, this technology still serves many markets and is the topic of continued research. A number of investigations will be considered in the next chapter.

Wire bonders work like sewing machines in that they rapidly "stitch together" IC's and substrates. Note that wire bonding offers some attractive features. First, the machines are fully programmable and therefore can accommodate variable IC sizes and bond pad locations. Lasky and Morovan emphasize this fact, because it minimizes the need for specialized (and expensive) tooling or jigs. Second, there is a certain amount of play within the wires that can allow for thermal expansion mismatch between the IC and the substrate.

Tape Automated Bonding (TAB)

According to Gileo, there are really only two ways to electrically connect a die: (i) by using wires or (ii) by forming a direct bond. Recall that wire-bonds are formed sequentially. Tape Automated Bonding or TAB is a wire bonding technology, but the wires are flat circuit traces. Most importantly, all the bonds are formed in a single step. This use of parallel processing can greatly enhance productivity (as mentioned by Lasky & Morovan). Of course, one can expect that the locations of circuit traces and bonding pads will be different for different IC's. With wire bonding, it is often possible to reprogram the machine to place a different number of wires in different locations. With the TAB circuits, one would have to retool with new masks, and tape window-making dies. This makes the TAB method less flexible.

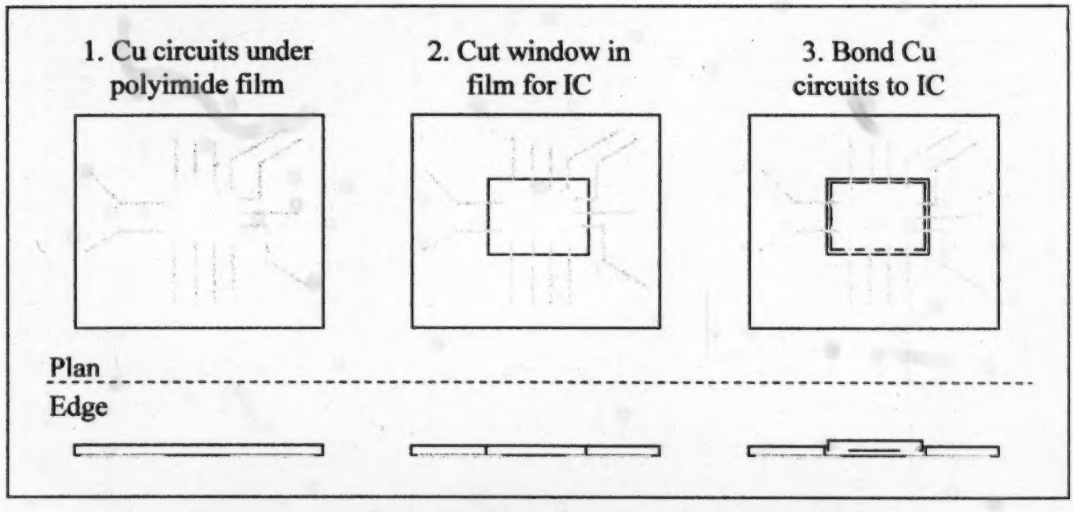

Figure 1-5 – Major process steps for TAB bonding. Note that the IC can be bare (Level I TAB) or prepackaged (Level II TAB). This drawing is based on descriptions from [Gileo 2002], [Lau & Mayer 1990].

Gileo describes the manufacturing process as a series of Cu TAB wires that are formed on a polymer film in a pattern that matches the die and extends outwards to other components. A hole is cut in the film that approximates the size of the die, leaving bare Cu wires that extend from the edge of the polymer film. They

are placed in contact with each other and then bonded using thermocompression. Figure 1-5 illustrates the concept.

The film is generally made from a continuous roll of polyimide (also used for photographic film), or sometimes even PTFE (Teflon®). Both have good physical properties and high service temperatures (>300°C). A cheaper, lower quality alternative is polyester. The films can be metallized on one or two sides, and may be laminated in order to accommodate extra layers of circuitry and reinforce the film for flexible circuit applications. With these flexible electronics, the polymer film is the PWB and either bare IC's or packaged IC's are bonded to the Cu wires. More on this is covered in Level II packaging methods.

Direct Chip Attach (DCA)

While important, both wire-bonded and TAB-bonded IC's have shown significant limitations, especially when it comes to packaging high-performance IC's. As seen previously, wire bonded and TAB bonded IC's are connected around their perimeters, and the lengths of wire used are fairly long in relation to IC component dimensions.

DCA technology addresses these issues by incorporating short (or "direct") electrical connections over the entire area of the IC. The purpose of this section is to review DCA design and fabrication, and consider the pros and cons of such an approach.

A popular form of DCA is the "flip chip". Note, however, that there are various DCA technologies, including some that employ TAB to obtain high density perimeter-style Level I connections on an area-array-style Level II substrate. These will be considered in the next chapter. Flip chip is basically a Level I packaging method wherein an IC die is placed face-down onto a substrate. Wires are replaced with direct conduction paths (using balls of solder or solder-coated bumps), and like TAB bonding, these paths are formed in a single step. Figure

1-6 illustrates the concept, and compares the area array approach against a perimeter array wire bond.

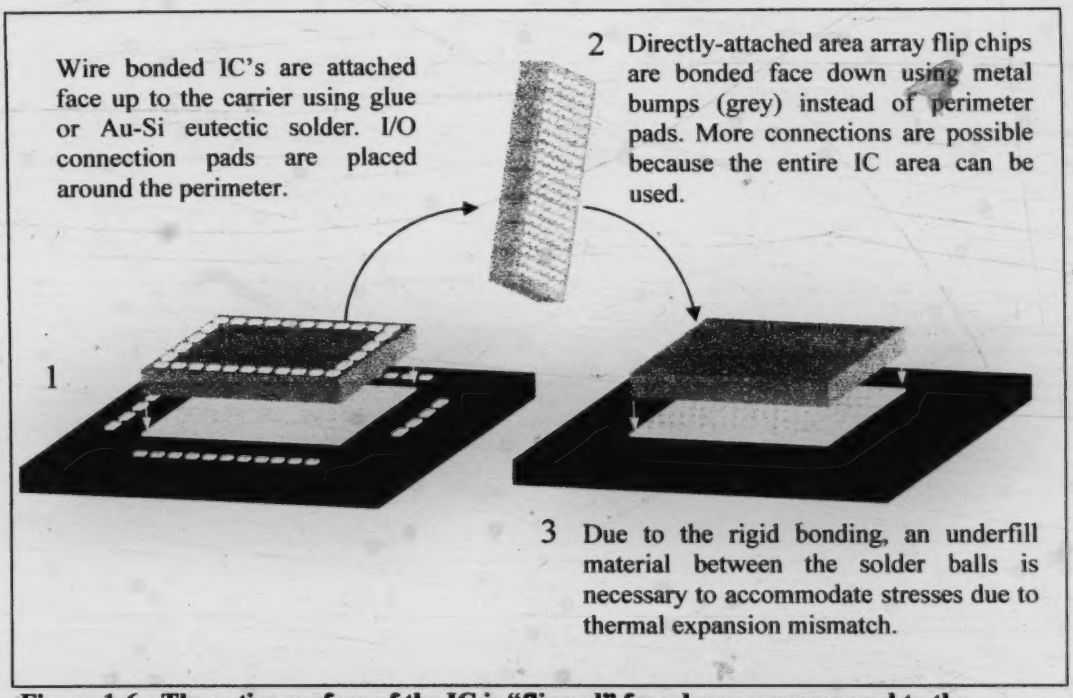
Wire bonded IC's are attached face up to the carrier using glue or Au-Si eutectic solder. I/O connection pads are placed around the perimeter.
2 Directly-attached area array flip chips are bonded face down using metal bumps (grey) instead of perimeter pads. More connections are possible because the entire IC area can be used.
1
3 Due to the rigid bonding, an underfill material between the solder balls is necessary to accommodate stresses due to thermal expansion mismatch.

Figure 1-6 - The active surface of the IC is "flipped" face down, as compared to the face up wire bonded configuration. The most important features of this Direct Chip Attach method is that the entire IC area chip can be used for connections to the carrier. Further, those connections are shorter than wires.

Limitations to the perimeter-based approach to wire bonding are a result of the fact that the wires must not contact each other, or a short will occur. The minimum obtainable pitch around an IC is about 60μm for a basic setup, which may be shortened to about 45μm if one uses staggered bonding sites [Cohn 2005]. Pitch is defined as the center-to-center spacing between interconnect bonding pads. Fine pitch wires can be as thin as 23μm diameter. Thin wires are more prone to sagging, so the interconnect distance is also very short. Area array package concepts allow for many more connections to be made using balls with much larger diameters.

While most Level I connection paths are made from Pb-rich Pb-Sn solder, there is pressure to find a Pb-free alternative in order to meet environmental legislation in Japan and Europe [Karim & Schetty 2000]. This seems to be a difficult problem to solve, however, and it may be that high-Pb alloys are the only viable choice for DCA connections. Possibly the biggest obstacle to overcome is the need for a high melting point solder that will hold Level I components together during a separate Level II soldering step. As will be seen, a much wider list of choices are available for lower-temperature Level II connections, including several Pb-free solder alloys and even conductive adhesives. Note that organic adhesives cannot be used at Level I, however. Gileo states that surface oxides which always appear on Cu and Al IC pads form an electrical barrier that the adhesives cannot remove.

For soldered joints, both the IC and the substrate have "pre-bumped" surfaces to which the bonding medium is attached. In a solder system, the bump includes conductive barrier layers that protect the Cu or Al pad on Si from being dissolved by the solder. These layers are referred to as the under-bump metallurgy, or UBM. The selection of UBM is an important feature, and different solder systems on the same UBM will interact in different ways. Examples of this and failure mechanisms that may result can be found in the literature, for example, [Suganuma, 2001], [Zeng & Tu, 2002].

Flip chip packaging offers many benefits, as outlined by Gileo and Blackwell. To start, the single step bonding method uses solder balls that are reflowed (i.e., remelted) so that they form a metallurgical bond between pads on the IC and bonding sites on the leadframe or carrier surface. Gileo reports that this technique was first developed by IBM in the late 1960's, who call their technology "controlled collapse chip connection," or C4.

Secondly, during DCA there are lower instances of IC damage. Recall that wire bonding is a mechanical source for vibrations and pressure. Gileo states that

solder reflow is a non-mechanical bonding method, so these potential damage mechanisms are eliminated.

Thirdly, face-to-face bonding greatly enhances the speed at which the IC's can communicate with other components. The direct bonds are very short, and this enhances performance by greatly reducing impedance (i.e., inductance, resistance and capacitance) effects.

However, there are also some drawbacks that make DCA a difficult technology to adopt. To start, Gileo remarks that assembly is complex. Direct chip attachment must be done in a more precise fashion than wire bonding or TAB. Further, if the DCA packages are incorrectly placed, reworking is usually not possible.

Wire bonding is called a compliant technology. This is because the electrical pathways (wires) are able to bend and accommodate thermal stresses. Recall that these stresses occur due to the fact that Si and carrier materials rarely have the same coefficient of thermal expansion. This is especially the case when cheaper epoxy carriers are used. Compliance greatly reduces bond failure. A major drawback of DCA is the fact that the short connections are rigid: they resist bending and are therefore noncompliant. In fact, the connections are so susceptible to thermally-induced failure that it is generally necessary to underfill the space between the IC, connections and carrier with an underfill material whose job it is to accommodate the stress. While the underfill may also help conduct heat from the IC, it represents a technically difficult and time-consuming production step.

Gileo states that the most common form of flip chip packaging is called "flip chip in package," or FCIP. In this embodiment, IC's are bonded in a level I fashion onto a carrier, underfilled and protected with a cover. These FCIP's are shipped to a board manufacturer who then uses Level II techniques to bond the packages to a PWB. A less popular (although functionally superior) method is

known as "flip chip on board," or FCOB (see also Blackwell, 2000). In this case, a bare IC is connected directly to a PWB. This can be very difficult for board assemblers to do, because it incorporates Level I DCA technologies (such as underfilling) that are not a natural component of Level II assembly.

Level II (Substrate to Board) Techniques

Overview

Level II packaging involves substrate to board (package to board, or carrier to board) manufacture and, over the past few decades, the way in which IC packages have been attached to PWB's has been changing. The main drivers are cost and performance. However, many of the old methods are still dominant in certain markets. The purpose of this review is to consider some of the most popular Level II packaging styles, and also to consider some of the products that benefit from each technology.

Through-Hole (TH) Component Mounting

Before the 1980's, the most popular method of electronic assembly was through-hole component mounting [Gileo 2002]. With this technique, the PWB contains electrically conductive holes (called vias) through which component leads are placed. The entire assembly is soldered using a wave process, as illustrated in Figure 1-7, below.

Wave soldering is still in use today, but the technology has changed [Manko 1986]. Often the boards move over a stationary solder wave. In addition, components can be mounted on both sides of the board. In this manner, both through-hole and surface mount devices (described later) can be soldered.

An example of a feed-through package is the dual-in-line package, as illustrated in Figure 1-1. According to Gilleo, the main benefit of feed-through mounting technology is its simplicity. Automation is easy, but not necessary since the process of plugging components in holes and wave soldering can be done

manually. Many low-cost, low performance devices are still assembled in this manner.

Wave Soldering Process:
A tank that contains molten solder is agitated so that a single ripple or "wave" is created on the surface. The wave is just high enough to contact package leads on the bottom of a PWB. Surface tension draws the solder upwards and forms a bond between the IC package leads and the PWB pads.

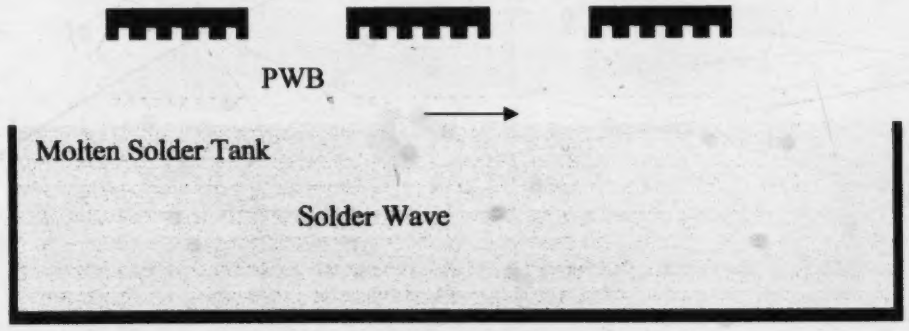

Figure 1-7 – Wave soldering process.

Beyond cost and simplicity, through-holes take up space that could normally be used by circuits buried within the board. Further, only one side of the board can be used. As a result, the procedure is not amenable to mounting large numbers of components in a small PWB area.

Surface Mount Technology (SMT)

SMT was developed in the 80's to replace feed-through packages, whose metal leads are fed through holes in the circuit board and soldered at the back. In contrast, surface mounted packages are soldered on the surface, and therefore do

not require through-holes. SMT devices can also be mounted on both sides of the board, and assembly can be automated.

SMT and through-hole assembly are compatible; a single PWB can be assembled using both methods. A simple way to convert a through-hole device (such as a dual pin array) is to simply fold the leads outward in a "gull-wing" to form feet. These feet may be surface mounted to the PWB, as shown in Figure 1-8. Such a configuration is easy to inspect, since all solder joints are clearly visible.

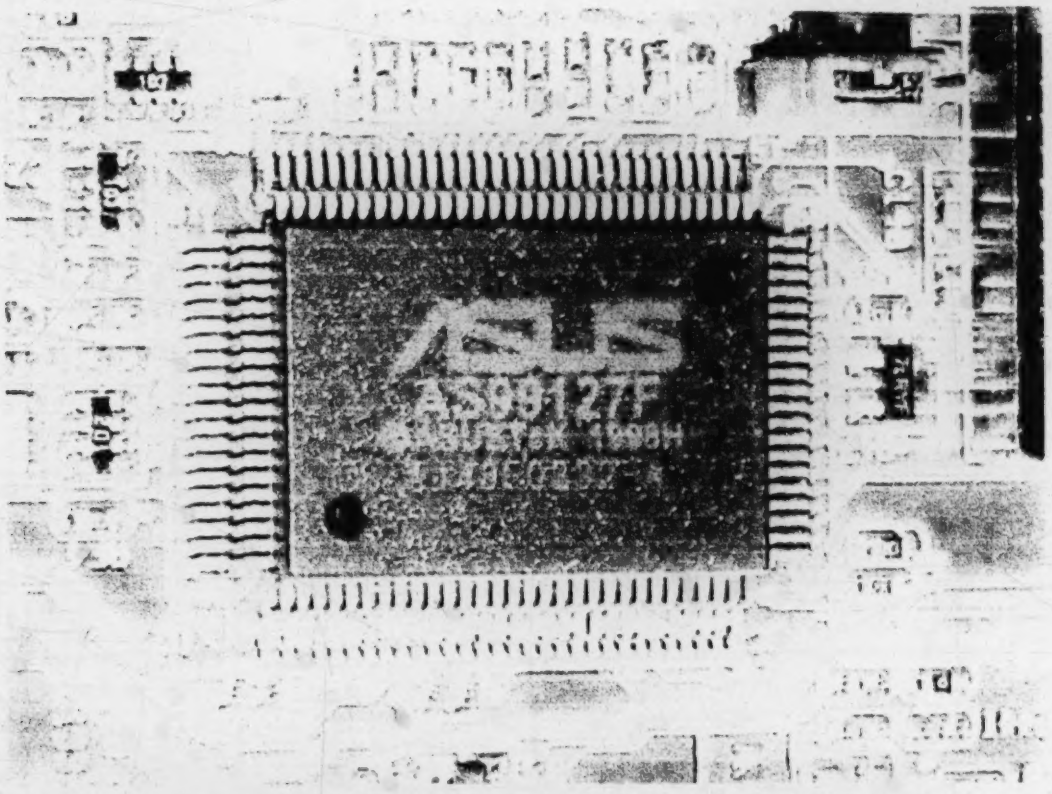

Figure 1-8 – The Quad Flat Pack (or QFP) is an example of an SMT device with leads around the perimeter. The leads are bent outwards, forming feet that are soldered to the surface of the PWB. Note, however, how much space is consumed relative to the dimensions of the black IC package. Photo by Olsen.

In the 1990's, the ever-growing numbers of input/output (I/O) leads on IC packages posed a problem. At a certain point, it became impossible to increase the number of I/O's by making these leads thinner. Also, surface-mount devices

such as the Quad-Flat Pack (or QFP, Figure 1-8) have leads sticking out from each edge, which makes its footprint much larger than the IC.

In response to these problems, Gilleo states that companies like IBM and Motorola began to reintroduce the old C4 technology that employed contacts on the bottom surface of the chip package, rather than simply around the edges. Motorola developed a cheaper version and called it the ball grid array (BGA). BGA's use solder balls that fit into a grid of IC pads on the back of the IC package. These balls are also bonded to the PWB surface. A well-known BGA design is the Ompack (or *Overm*oulded package). The Ompack is a plastic BGA (or PBGA). In this case, the carrier and IC encapsulant is made of a polymer.

Recall that this is Level II (carrier to board) packaging. The IC itself may be bonded to the carrier using a variety of techniques, including wires or smaller solder balls to form a Level I BGA. In either case, the Level II package is its own entity. That said, the type of Level I packaging used may influence the overall package size. Figure 1-9 (below) is a drawing of two types of IC's bonded to a Level II area array carrier. Note that both IC's would normally be covered with an encapsulant.

Minimalist Packaging

The term minimalist packaging refers to use of Level I DCA (flip chip) in order to create a Level II Area Array SMT device whose package dimensions are as small as possible. In Figure 1-9, the drawing on the right depicts a minimalist package using the flip-chip design. Another term called CSP (Chip Scale Package) is also used. However, by definition a CSP must have package dimensions that are no larger than 120% of the width and length of the bare IC.

According to Gilleo, DCA (flip chip) is the simplest and most minimal package available. The connections are made through metal bumps that are formed on the face of an IC. The chip is then "flipped" face-down and bonded to the opposing

face of the circuit board. The solder balls may or may not be made completely of solder, either. In the original C4, most of the ball was solder-coated Cu.

In the simplest DCA configuration, however, the bumps are made entirely out of solder. This approach is very similar to Level I DCA, and the thermal coefficient of expansion (TCE) difference between the IC package and the polymer composite PWB is large. As before, the TCE mismatch between the Level I package and the PWB is a source of solder bond failure, and therefore an additional polymer composite underfill is used. The underfill forms a stronger bond and serves to accommodate the thermal expansion stresses.

Between the solder and the IC substrate is a bonding pad. Another pad is found between the solder and the PWB. These pads contain one or several layers of conductive material whose job it is to serve as a bonding site and a diffusion barrier for the solder. The makeup of the pad is known as Under Bump Metallurgy, or UBM. More about this will be discussed later.

As mentioned, DCA devices are the best-performing, with minimal amounts of performance-robbing impedance and minimal size requirements. Up to 7800 bumps [Gileo 2002] are available. Note also that the solder balls can exhibit a larger pitch than perimeter-style leads and still contain a larger I/O count between the package and the board.

An interesting article was published last year [IBM 2004], where IBM announced the development of a Pb-free version of C4 technology. It is called C4NP, and NP stands for "New Process." The technology allows a manufacturer to "screen-print" molten alloy as solder balls directly on Si wafers. C4NP is a wafer level packaging method that offers a productivity gain through parallel processing. In this step, the parallel process would be the deposition of all the solder balls in a single step for any size of wafer. Wafer level packaging is discussed in more detail later.

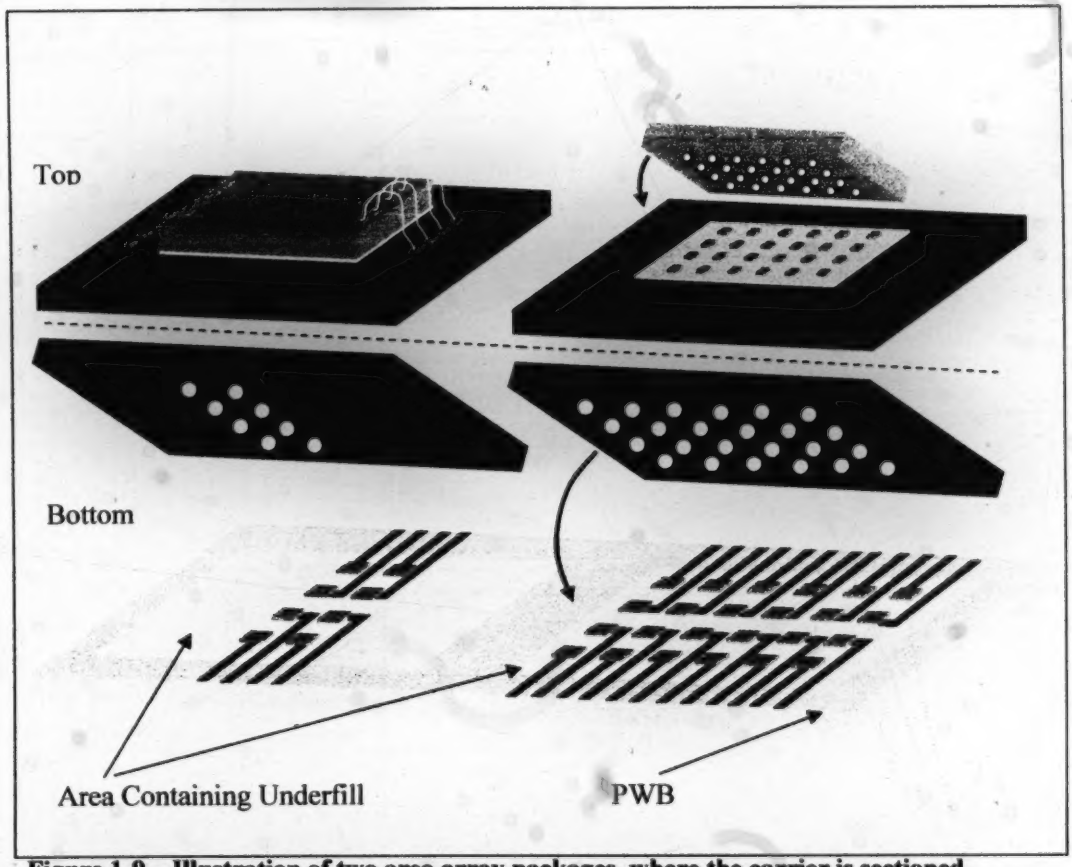

Figure 1-9 – Illustration of two area array packages, where the carrier is sectioned in half in order to show both sides. *Left*: The Level I packaging style is gold wire bonding from 8 perimeter pads on the IC to 8 perimeter pads on the carrier (top view). The Level II packaging style is a 2x4 area array-style SMT using solder balls. *Right*: The Level I packaging style is DCA (Direct Chip Attach) using a 4x6 area array with underfill. The Level II packaging style is area array-style SMT using solder balls. *Both*: The pads and solder balls on either side of the carrier are connected by internal circuits.

Pin Grid Array (PGA)

Another Level II technology is called the Pin Grid Array (Figure 1-10). In this case, an IC package is made in a fashion similar to the BGA, except that pins are used. Further, these pins are soldered only to the IC package. The PWB has a plate soldered to it that accepts the PGA. In a sense, it is a removable package that plugs into or out of the board. An example of a PGA device is an upgradeable Intel® Celeron® CPU.

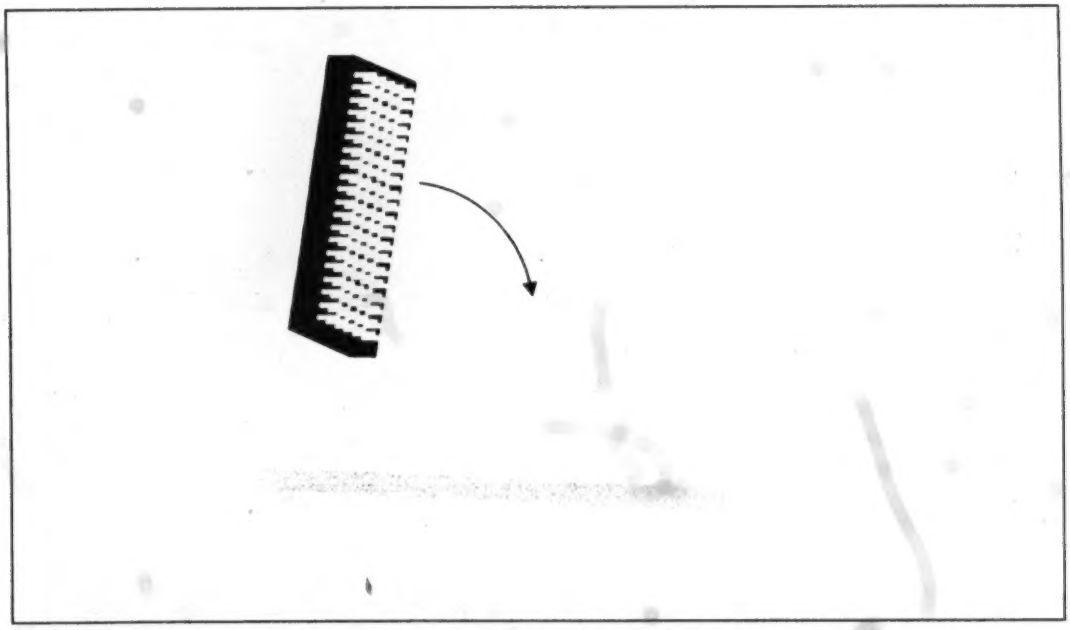

Figure 1-10 – An IC package (black) can be bonded to a PWB by means of a Pin Grid Array (PGA). In this case, there is a socket that is surface mounted to the PWB. Based on Fig 15.7 from Mayer and Lau, 1990 and descriptions from Gileo.

Pb-Based Solders

Overview

Most Level I and II connections are bonded using metallic solders that contain Pb. While the entire list of Pb-containing solders (and Pb-free alternatives) for electronics is large, [Bastow 2003] neatly categorizes them into five categories. His work is summarized here:

Sn-Pb: These are generally used with compositions close to the 60Sn-40Pb eutectic. They melt at around 185°C, and are the backbone of electronic solder technology. They are also relatively inexpensive and have a well-established database of properties.

Pb-free: Categorized by Bastow as compositions that are mainly Sn based. The Sn-Ag-Cu-X family as a favourite, though the topic is discussed later.

In-Pb: In this class of solders, In is used instead of Sn for applications (such as optoelectronics) that require thick Au metallizations. This is because In is reportedly less prone to dissolve Au than Sn.

High-temperature: These solders typically contain 90% or more Pb, and melt at temperatures around 300°C. High temperature solders are typically used in Level I applications. They also represent a problem for the Pb-free movement, although a high melting-point alternative may be 80wt%Au-20wt%Sn [A. He et al, 2002]. This alloy is currently used in optoelectronic and MEMS packaging. A less-developed alternative is Sn-rich Au-Sn solder [Lee & Chuang 2003].

Low-temperature: These are designed for use with temperature-sensitive components, and generally have good ductility. After Level I bonding, the packaged IC will then be soldered to a PWB in Level II. Low-temperature (and Sn-Pb eutectic) alloys can be used here so that the Level I solder bonds do not remelt.

Brief Review of Sn-Pb Solder Theory

This section is a review of how Sn-Pb solders work, and typical characteristics of a solder joint. It is based on a summary by A. Rae from Cookson Electronics [Rae 2002].

Solder can be applied by a number of methods, although the application of paste is quite popular. Solder paste is also called ink, and is comprised of small solder spheres in an organic carrier. The paste is applied using a screen printing method, which will be described later in the thesis.

Solders form bonds by growing intermetallic compounds between the two joining surfaces. When the system is Sn-Pb and the surfaces are made from Cu, the intermetallic compounds (or IMC's) are based on Cu-Sn. IMC growth is diffusion-controlled, and its rate is proportional to the square root of time.

As is expected from thermodynamics, the IMC composition will vary across the solder joint. Cu-rich phases (such as Cu_6Sn_5) can be expected near the Cu surface, while almost pure Sn-Pb will exist in the middle of the joint. The presence of surface oxides on the Cu will greatly affect solderability, which is tied to the rate of initial IMC growth.

Rae stresses that while it is important to form an IMC layer, the thickness and composition are critical factors in determining bond integrity. For example, a poor solder joint will exist if the IMC layer is too thick, or if IMC layers are composed of the wrong phases. Phase morphology also plays a role, and certain features are typical of solder composition. For example, a solder with high Pb content will exhibit a needle-like microstructure. Solders with high Sn have finer structures, and may have a thicker IMC layer due to the affinity of Sn for Cu.

For Sn-Pb, an IMC layer thickness between 1 and 5μm is deemed acceptable, although the shape and distribution of the IMC particles (or phases) that make up the layer are just as important. This is because IMC's are generally harder and more brittle than the alloy matrix, so they can either reinforce the joint or serve as crack initiation sites. The topic of Sn-Cu IMC's is discussed further in Chapter 4.

Rae discusses several important parameters for any soldering system. These include the free energies of the solder components relative to the joining surfaces. Temperature, duration of processing and environmental considerations also come into play. Variables such as humidity and oxygen content are important before, during and after processing.

Pb-Free Solders

Pb-Free Solder Compositions [Hwang 2005]

According to iNEMI, the most favoured Pb-free solder compositions are Sn-Ag-Cu for reflow and Sn-Cu for wave soldering [iNEMI, 2004]. The Ag-containing alloy offers the best balance of properties, while the Ag-free alloy is cheaper. Aside from these, however, there is a large number of other alloys to choose from.

For example, [Fukuda et al 2003] discuss a variety of alloys that are in use by Japanese industry.

Table 1-1 – Summary of Sn-Alloying Elements for Pb-Free Solders

Element	Properties
Ag	• Forms an eutectic with Sn at about 3.5% Ag. • Greatly enhances strength and forms Ag_3Sn intermetallic. • Expensive.
Cu	• Forms an eutectic (T_m=227°C) with Sn at about 0.7%Cu. • Enhances strength, but reduces ductility and fatigue resistance. • Forms Cu_6Sn_5, which is good for solderability, but can also form Cu_3Sn (see chapter 4) at high temperature, which reduces solderability.
Bi	• Bi greatly lowers the melting point of Sn. • Below 1%, Bi forms a solid solution with Sn. • Above 1%, Bi precipitates out of solution as a brittle secondary phase. • Additions must be kept to below 5%, or ductility is compromised. • Other references [e.g., Bastow 2003] state that Bi is prone to Pb-contamination, since it forms a low melting-point eutectic at ~90°C. • Nontoxic.
In	• Greatly enhanced fatigue resistance. • Strongly lowers melting point. • Forms substitutional sold solution with Sn and intermetallic compounds (IMC's) with other alloying elements, for example $AgIn_2$ and CuIn. • In strengthens Sn alloys. • Expensive, with cost similar to Ag.
Ga	• Lowers the melting point of Sn. • Enhances fatigue strength. • Reacts with In to form finely dispersed Ga particles that further enhance fatigue strength.
Zn	• Very inexpensive element. • A possible, though unpopular candidate material, due to oxidation (solderability) issues [Humpston & Jacobson 2004].

Nearly all Pb-free candidates are almost pure Sn. This is because Sn is relatively inexpensive, plentiful, and its properties are well-known. Some drawbacks of

high-Sn alloys include problems with whisker formation.[2] Whiskers are single-crystal, dendritic growths of pure Sn that occur as a mechanism for stress relief. Table 1-1 is a summary of some popular alloying elements for Sn-based Pb-free solders, based on descriptions in [Hwang 2005].

Hwang offers two ways to consider replacing Pb. One is called the *drop-in* approach, while the second is called the *modification approach*. Each is separated by an accepted processing temperature, which happens to be 235°C for reflow and 245°C for wave soldering. Below these temperatures, a drop-in approach must be adopted. Above these temperatures, a modified approach is in order. Note that during reflow, a flat solder bump (deposited by electroplating or screen printing) is heated until surface tension effects allow the metal to form a ball-shape.

Table 1-2 – Pb-Free Solder Summary, based on [Hwang 2005]

Alloy (wt%)	Pros	Cons
88.5Sn-3.0Ag-0.5Cu-8In	Low process temp (<205°C). Exceptional fatigue resistance.	In and Ag are expensive at ~US$150/kg, (Sn is ~US$8/kg).
95.4Sn-3.1Ag-1.5Cu	Very good fatigue resistance. Absence of In lowers the cost.	High process temp (>215°C)
97.3Sn-0.7Cu	Highest process temp. Inexpensive (Cu is ~US$2/kg). Very low toxicity.	Poor fatigue resistance. Poorer solderability than Pb-Sn.
63Sn-37Pb	Lowest process temp. Good fatigue resistance. Good solderability. Least expensive.	Pb is being banned for electronics use in Japan and Europe.

With the modification approach, one employs the iNEMI choices. In the case of reflow work, an eutectic or near-eutectic Sn-Ag-Cu system offers a more environmentally-friendly choice with enhanced physical properties over Pb-Sn.

[2] See for example www.inemi.org for information on Sn whiskering.

With the drop-in approach, often the Sn-Ag-Cu system is modified by additions of In and Bi, which serve to significantly lower the melting point while enhancing solderability at lower processing temperature. A low melting point solder can contain high amounts of In, which makes this alloy expensive. However, the fatigue resistance of such alloys can be >6 times better than Pb-Sn. Table 1-2 outlines some notable Pb-free solders, and compares them with eutectic Pb-Sn.

Solder Fluxes

This review will focus on Sn-based solders, and is based on descriptions by Humpston and Jacobson [Humpston & Jacobson 2004].

The purpose of a flux is to clean the surface of two metals that are to be soldered. Cleaning generally refers to the removal of dirt and surface oxides that hinder wetting. In the case of electronics, the surfaces to be soldered are normally Cu, and the solder is mostly composed of Sn. Electronic parts also tend to be kept relatively clean, so that the fluxes employed do not have to be overly aggressive. Sn-based systems that contain Zn and In need to be treated with different types of flux, however.

The authors go on to describe two main classes of Sn flux: those that require cleaning and those that do not. The first class contains at least four main ingredients. First, there must be a component that removes the oxide or dirt, such as an acid or halide. Second, the flux requires a chemical that will be in a liquid phase at the melting point of Sn. This chemical must form a protective barrier so that the Cu does not reoxidize. Third, there must be a surfactant present that will enable the barrier chemical to wet the Cu. A final chemical is added to tailor the rheological characteristics of the flux.

Finally, a commonly used "must clean" flux for Sn is called Rosin. It contains a carboxylic acid called abietic acid. The role of the acid is to convert copper oxides into compounds that can be easily removed from the surface by cleaning – hence the name.

The second class of flux does not need to be cleaned. Humpston and Jacobson state that a "no clean" flux simply produces reaction products that are considered benign, and therefore can be left on the PWB or other surface. There are two ways to convert the surface oxide into benign substances. The first is to use a "must clean" flux chemistry, but dilute the active ingredients so that only a limited amount of products form. The second approach is to polymerize the products in some way. The authors give an example of gelatin, which simply encapsulates the products and leaves it on the part surfaces.

Section 2: Electronic Materials R&D

Introduction

The purpose of this chapter is to look at the way electronics packaging technology is changing, and what the drivers for change are. To begin, an overview of European legislation to restrict hazardous materials is given. Next, various R&D works in Level I interconnects are reviewed. Finally, Level II innovations are discussed, with emphasis on Pb-free and packaging technologies that span both Level I and II domains.

WEEE and RoHS Legislation

In Europe, the push for Pb-free adoption falls under two legislative bodies: WEEE and RoHS. This summary is based on a comprehensive review by Dionics, found at www.pb-free.info. Note that Japan has its own environmental laws. More on this topic can be found in [Fukuda et al 2003].

WEEE stands for Waste Electric and Electronic Equipment while RoHS stands for Reduction of Hazardous Substances. Both are separate pieces of legislation that apply to producers of electric and electronic equipment (EEE) within the European Union and those producing EEEs for import into the European Common Market. WEEE deals with setting minimum levels of recycling, with the understanding that non-recycled materials will eventually end up in land fills. RoHS addresses one of the most troubling consequences of handling and also land-filling EEEs. This is exposure to and the introduction of mercury, lead, cadmium, chromium VI and two bromine-containing substances named PBB and PBDE[1] into the environment.

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[1] PBE = Polybrominated diphenyl ether, PBB = polybrominated biphenyl

The RoHS list that defines such substance-containing products is taken from the WEEE directive, although RoHS reportedly allows some exemptions. For example, Hg is allowed for use in light bulbs and all hazardous substances are allowed for use in military products. In addition, RoHS has been written so that the list of restrictions can grow in the future. Such restrictions are to be based on scientific evidence, and a "precautionary principle" is employed that puts the onus on manufacturers to demonstrate that the materials used in EEEs are safe.

Finally, it is noted by Dionics that parts of the legislation are ambiguous. From sources such as the Advanced Packaging website [http://ap.pennnet.com], it is apparent that the ambiguities have not been settled, especially concerning the allowed uses of Pb in EEEs. Note that RoHS comes into effect July 1, 2006.

In a web article by [Groover 2005], the ultimate goal for lead-free electronics is a reduction of Pb concentration to less than 1000 parts per million. As mentioned in Chapter 1, this is not expected to happen for Level I flip-chip connections, where high-Pb (i.e., high melting point) bumps used to solder the IC to the carrier are the only viable alternative. In this case, the EU is reportedly suspending the Pb-free restriction until a later date. One other option may be the widespread adoption of flip-chip on board (FCOB), which can be used with lower melting point solders [Baldwin and Higgins 2005]. This will be considered more fully later in the chapter.

Groover goes on to explain the implications of Pb-restrictions on packaging. In addition to Pb-free solder, Pb-free packaging needs to address two other challenges. First, electronic boards must be capable of surviving higher temperature reflow operations (between 245 and 260°C). Second, for leadframes that are usually finished with Pb-Sn, the Pb must be eliminated here as well. The author notes that in Q2 2004, approximately 88% of leadframe products were finished using Sn-Pb, while the balance used Sn-Bi (3%), matte Sn (4.7%) and Au over Pd over Ni (NiPdAu, 4.3%).

As mentioned previously, RoHS goes beyond Pb restrictions to dictate a vision for safe, "green" packaging. Groover, who is a VP of Amkor Technology Inc., sees green packaging as a much greater challenge. For example, flame retardants used in epoxy-based IC encapsulants typically contain As and Br, while solder mask materials and polymer substrates contain halides. All these substances must also be eliminated (and viable substitutes found) in order to make electronics green.

Developments in Level I Connections

Overview

This section will highlight some examples that show how IC dies are being packaged more efficiently in order to continually improve interconnect densities and semiconductor utilization values per unit of board space. As will be seen, older techniques such as wire bonding have the potential to see continued use in state-of-the-art applications. In other areas, cost benefits are realized when packaging steps are performed on IC's while they are still part of a wafer.

Wire Bonding (WB)

Enhancement of wire bond reliability is still a topic of research. [Ker & Peng 2002] consider a redesign of IC bonding pads that replaces a stack of monolithic vias under the bonding pad with a stack of smaller via arrays. The effect is to roughen the pad surface, which increases adhesion. They also optimize the pad layout in order to improve bond quality and electrical performance without adding to manufacturing costs.

If the bonding forces (e.g., ultrasonic vibrations) are too aggressive, one can expect an increased risk of IC damage – especially for devices that are located near the bonding pads. According to [Binner et al 2004], this is especially true for IC's that incorporate low-dielectric (low-k) materials. Low dielectrics replace conventional SiO_2 in between the IC circuits in order to lower impedance and enhance signal speed. Binner et al state that these low-k materials tend to be very

weak, and they have investigated a new wire-bonding system. The results are mixed, however, and the need for further research is identified. Recall that in the previous section on DCA, it was mentioned that direct solder reflow had the advantage of no applied stress during solder bonding. This advantage looks to be of increasing value with high-performance IC's.

As mentioned, Au and Al are the materials of choice for wire bonding. [Khoury et al 1990] have investigated the use of Cu as a superior alternative over Au. In this case, both Au and Cu wires were bonded using Ag-filled epoxy which was cured at elevated temperatures. Advantages included better bonding (due to higher strength), the ability to bond directly to Cu interconnects (i.e., Cu lead frame) instead of Ag-plated Cu, and higher conductivity with comparable bond reliability. Disadvantages included the need for a $95\%N_2/5\%H_2$ environment (to limit oxidation) and higher operating temperatures.

Wire bonding still has a bright future, and possibly the most exciting development is in 3D packaging. A review is given later, based on the work of Lee Smith from Amkor Technology, Inc. [Smith 2002].

While the information may be dated, [Okikawa et al 1989] have considered the advantages of electrically-insulated wire bonds as an enabling technology for higher wire density and greater yield. They have mentioned significant patent activity by researchers. Their method of choice involves selection of a coating that will burn off locally at the point of solder ball formation. The coating should also be easily removed during ultrasonic formation of the wedge bond. In the end, a polyurethane material was selected for the purpose.

Still another approach to increasing interconnect density is through staggered bonding pads [Cohn 2005]. According to the authors, the substrate-side pitch can be reduced from about 60μm to 30μm. Note that a concern with any wire-bonded die is that the wires can deform and contact each other, forming shorts. This can be especially troublesome during transfer molding of an epoxy resin encapsulant.

Transfer molding is also described by [Cohn 2005]; it is essentially an injection moulding process that forces a thixotropic resin into a chamber over top of the IC and substrate. A thixotropic fluid is a substance whose viscosity drops under shear forces. In this instance, the transfer moulding process enables a relatively thick resin to flow more easily into the chamber cavity, enabling faster fill times and lower chances of wire deformation.

Tape Automated Bonding (TAB)

In the field of TAB, progress is being made with flexible circuitry. Flex circuitry has similar elements to TAB, and is an enabling technology for devices like hard disk drives [Buetow 2004]. In an article from Advanced Packaging, [Pacual & Calender 2004] used a combination of flip chip packaging and flex circuits to develop an ultra-small biomedical device. No metallic solder was used, but rather a combination of conductive and nonconductive adhesives. As with conventional TAB, the flex circuitry is built on polyimide film.

Some of the more recent developments use TAB in DCA packaging. These include the micro-BGA (or μ-BGA). This technology spans both Level I and Level II techniques, and will be discussed later.

Wafer (or IC) Bumping Technologies

All IC's must be prepared for Level I interconnection. This involves the deposition of contact layers that allow high performance signal conductance, while ensuring a cost-effective and reliable bond to the substrate. This section gives an introduction to a technique called bumping, which is used for flip-chip bonding.

According to [Baldwin & Higgins 2005], IC bumps serve four functions. The first two are for electrical and mechanical connection between the IC and substrate. The third function is to conduct heat away from the IC. Finally, IC bumps protect the IC interconnect pads from the outside environment. All

functions are met by a series of layers that make up the under bump metallurgy (UBM), as described in Chapter 1.

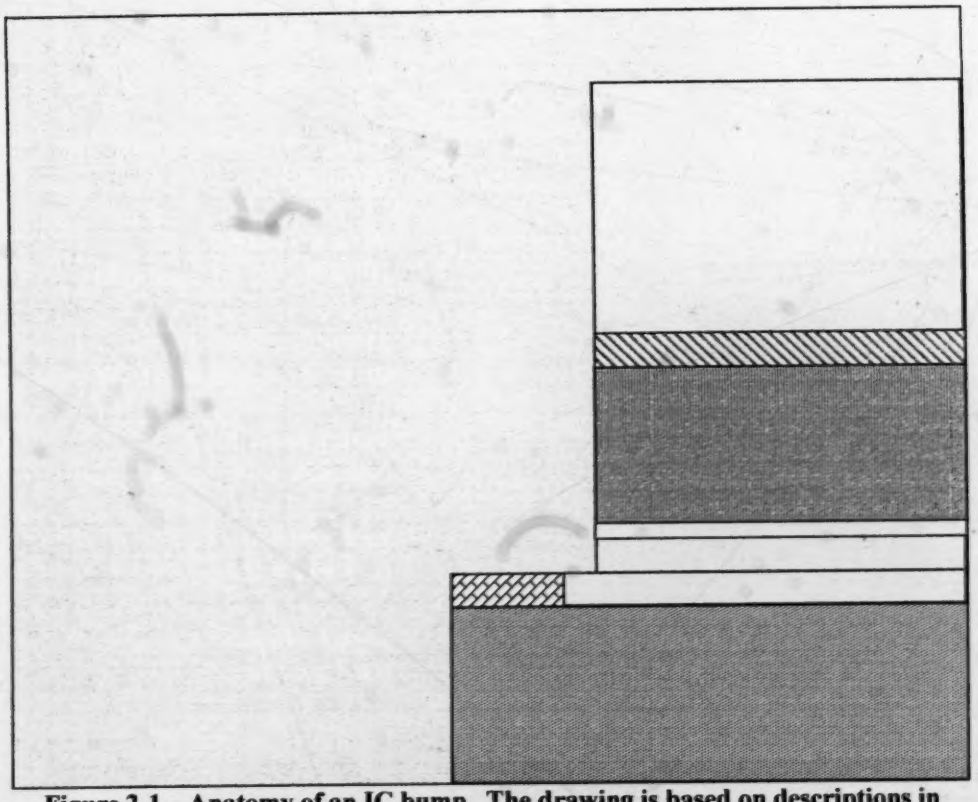


Figure 2-1 – Anatomy of an IC bump. The drawing is based on descriptions in [Okikawa 1989] and [Baldwin & Higgins 2005].

A very popular technique for forming bumps on IC pads is electroplating, although evaporation and screen printing techniques are also used [Blackwell 2000], [Baldwin & Higgins 2005]. [Okikawa et al 1989] use an electroplating method to build up Cu bumps on an IC surface. A schematic of the bump, including UBM is shown in Figure 2-1, although typical materials reported by Baldwin & Higgins are also shown.[2] In the Okikawa study, the formation of Sn-

[2] The authors also give a number of typical metallization systems, which are denoted starting with the adhesion layer and working upwards. These include [Cr, Cr-Cu, Cu, Au], [Ti, Ni, Au], [Ti, W, Ni, Au], [Al, Ni-V, Cu] and [Zn, Ni, Au], and are qualified for use with various solders.

Cu intermetallics on a more basic UBM (i.e., no adhesion layer, a TiW diffusion barrier, and electroplated Cu on a sputtered Cu starting layer) is analyzed. It was found that the surface roughness of the Cu bumps (as determined by plating current density) has an effect on the properties of the Sn-Cu IMC's and therefore the integrity of the solder bond. Baldwin & Higgins note the importance of a good UBM, since this has a direct effect on reliability due to thermo-mechanical stresses.

Other, more exotic IC bumping technologies also exist. An interesting approach is given by [Yang et al 2003], who deposit molten drops of solder in a process they call Jet Bumping. Similar references are given in Baldwin & Higgins.

Wafer Level Packaging

A great deal of research is being conducted in the DCA flip-chip field. [Tay et al 2004] look ahead to 2009, when experts predict a ball-grid pitch of 100 μm. This sort of scale is part of a new type of Level I packaging technology known as wafer-level packaging. One of the main benefits of this technique is a significant reduction in process steps, from 1 million steps per 1000 chip wafer to only a dozen. Such a reduction is possible by processing all the IC's at once while they are still part of a wafer.

The authors consider three different styles of Level I interconnect that will allow for the required denisty, while accommodating thermal expansion stresses and electrical impedance requirements. Their styles include a "bed of nails" interconnect which is compliant, a stretched solder bond which is semi-compliant, and finally the use of non-compliant (i.e., rigid) solder balls that do not require an underfill. In all cases, these interconnects are to be Pb-free and are designed to meet the expected electrical performance criteria for 2009.

3D Packaging

In Chapter 1, the differences in scale between IC-level and PWB-level features were described. It was also noted that the scale continues to widen. While there

are efforts underway to integrate more functionality on a single chip [Gupta & Gupta 2003], [Yanagawa 2004], there exists an opportunity to increase functionality on the board as well.

The approach is outlined by Lee Smith of Amkor Technology [Smith 2002], and his work is summarized here. It is now possible to increase IC functionality and board functionality by stacking IC's and IC packages one on top of the other. The approach has pitfalls, including complex manufacturing [Cohn 2005] and problems with thermal management, but for certain applications it has become an enabling technology.

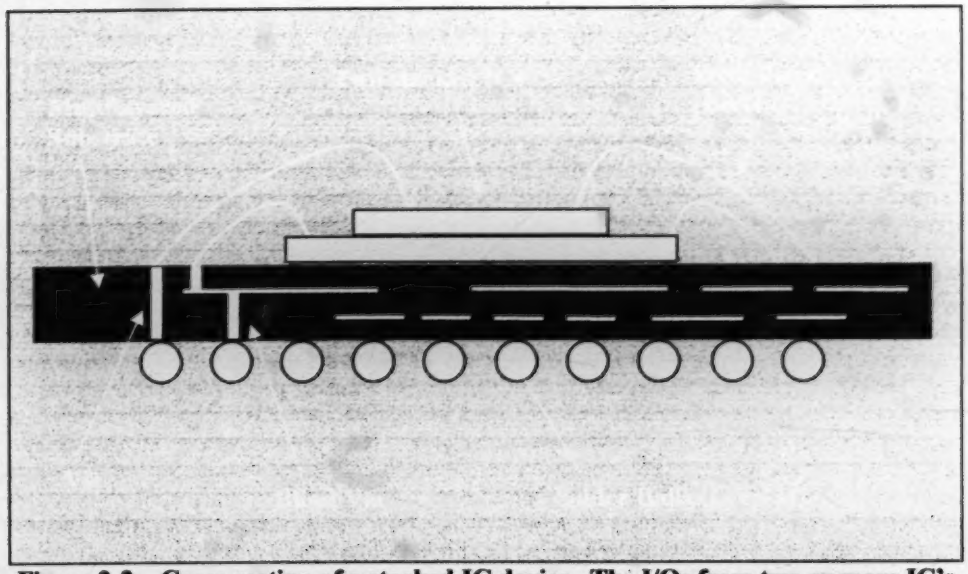


Figure 2-2 – Cross-section of a stacked IC device. The I/Os from two or more IC's can be efficiently carried by an area array SMT substrate to a PWB without having to integrate both IC's into a single die. The drawing is based on Figures 5.6, 5.11 and 5.17 of [Smith 2002].

Developments in Level II Connections

Overview

Level II packaging is the focus of a great deal of research. While a comprehensive overview is beyond the scope of this thesis, a few interesting topics will be presented in this section. To start, a popular packaging technology known as micro Ball Grid Array (μ-BGA) is reviewed.

Micro-Ball Grid Array Packaging (μ-BGA)

This section is a summary from [Fjelsted et al 2002]. μ-BGA is a packaging method that has become popular for applications such as Flash™ memory, and is probably best described as a combination of TAB and ball-grid DCA. Within the context of this thesis, the reader can think of μ-BGA packaging as a combination of Level I and Level II design.

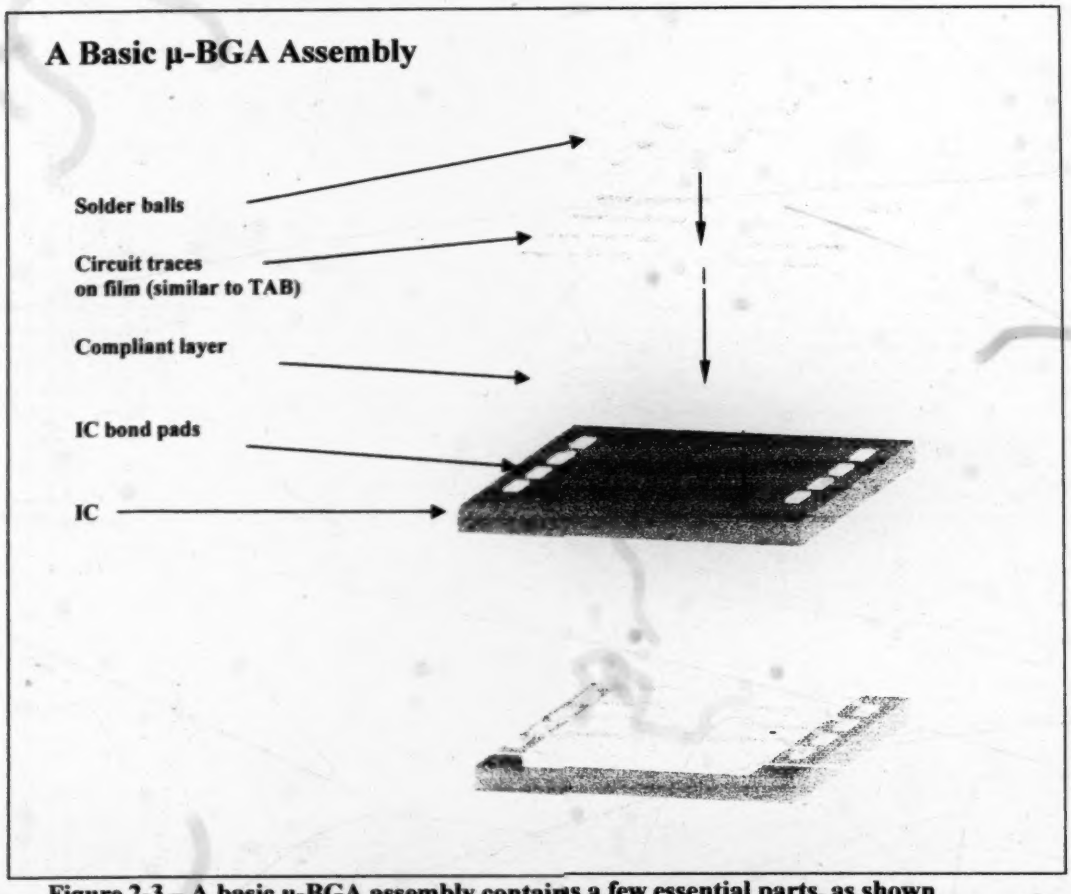
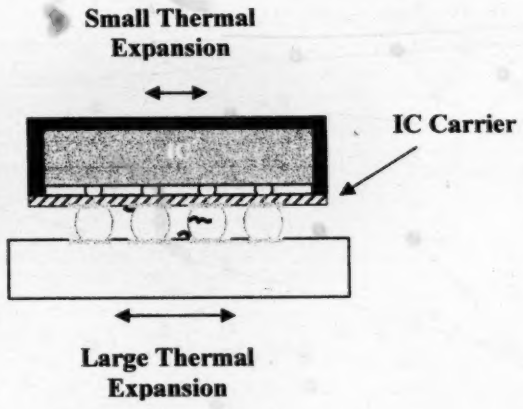


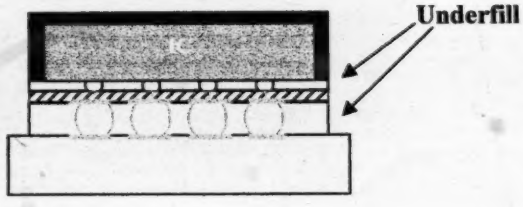
Figure 2-3 – A basic μ-BGA assembly contains a few essential parts, as shown above. In this example, the wires are TAB-bonded to the IC.

As will also be seen, many new innovations are focused on the use of Pb-free materials, and four major applications will be discussed. The first is as a finish in

Area array packages have short conduction paths. During use, thermal stresses build up and typically lead to solder failure between the IC substrate (hatched) and the PWB.



As is done between IC and carrier (Level I), underfill (dots) is added between the substrate and PWB in order to help the solder accommodate the stress. Underfilling is an expensive procedure.



µ-BGA takes many forms. This newer version connects area-array IC pads to area-array contacts on the PWB. The IC is packaged with a compliant material that holds compliant TAB-bonded interconnects between the IC pads and solder balls. Underfill between the IC package and the PWB is no longer required. See [Ker & Peng 2002] for a discussion on manufacturing methods.

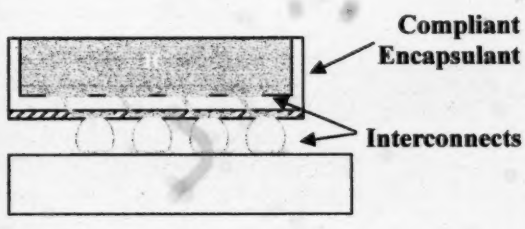


Figure 2-4 – DCA BGA (Level I and Level II) versus µ-BGA.

PWB contacts. The second is for solders that are used to connect the PWB contacts to component leads. The third is a solder-free approach that uses Au-bumps and adhesives to bond an IC substrate to a PWB. The final application is as a finish for the component leads, which are of course attached to the IC package. An example of lead-free component finishes on phosphor bronze component leads is highlighted.

The μ-BGA design addresses problems with thermal expansion mismatch in a way that does not require the use of an underfill. Recall that underfilling is an undesirable process for Level II assemblers. μ-BGA is classified as a chip scale package (or CSP), which means that the carrier length and width are less than 20% larger than the die. It is a foundational technology in Flash™ memory and RDRAM, which is a future computer memory format. Developed by Tessera Inc., μ-BGA is used under license by many other companies, including Intel, Hitachi and Sony.

A basic μ-BGA assembly is shown in Figure 2-3. This design allows for thermal coefficient of expansion (TCE) mismatch to be absorbed by the flexible leads and flexible (or compliant) layer. While there are many designs, the basic embodiment seems to be the use of a compliant (or flexible) connection between the IC bond pad and the solder ball. In the example of Figure 2-3, the solder ball contacts are fanned inward relative to the IC contacts.

The fan-in configuration is beneficial, because future versions of the IC are typically smaller (die shrink) and yet the matching pattern of solder pads on the PWB can remain the same. Since the solder balls are sitting on a compliant layer of material with compliant interconnects, this design allows them to move vertically as though they were springs. This feature is important because it

ensures good contact, especially if the manufacturer wants to test the package[3] before assembly onto the PWB.

Note that in Figure 2-3 the IC only has bonding pads on its perimeter. There are several generations (and variants) of μ-BGA technology whose purpose is to reduce cost and tailor the design to different configurations. One example is shown in Figure 2-4, where an IC with an area array of bonding pads is connected to the surface of an area array of contacts on a PWB. Figure 2-3 also illustrates how the use of a Level II underfill is avoided.

Flip Chip on Board (FCOB)

The following description is based on Baldwin & Higgins. It represents a typical FCOB assembly process. Other descriptions are available in the literature, including [Gileo 2002].

FCOB is a technology that skips the step of mounting an IC on a carrier within a Level I package. Instead, an IC is bonded directly onto the PWB in order to gain a performance and cost advantage. As with μ-BGA, it can be thought of as a technology that spans both Level I and II packaging. While Level I flip-chip interconnections tend to use high melting-point (typically high-Pb) solders, the FCOB technique is compatible with lower melting-point solders. This is a major advantage, since there it opens the door to a variety of Pb-free solder options.

FCOB has some drawbacks, however. To begin, there is the problem of attaching a low-thermal expansion IC with a high-thermal expansion PWB. Further, because rework is often difficult or impossible, one must ensure that both

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[3] This is an issue referred to as "Known Good Die" [Gileo 2002]. Since rework (or reassembly of nonfunctional boards) is costly, a manufacturer will want to test the electrical performance of IC packages before they are connected to a PWB. Of course, a good test requires good contact between the IC and the probes. Testing a set of spring-like contacts makes it easier to ensure that there is good contact with the probes, while minimizing the risk of damage due to probe pressure.

the IC and PWB are defect-free. This is known as "Known Good Die" and "Known Good Board," and is discussed in more detail elsewhere.[4] The expansion problem is solved by underfilling with a material that bonds the IC to the board. As mentioned in Chapter I, this underfill accommodates the stresses due to thermal mismatch and greatly reduces the rates of thermo-mechanical failure, but it is an unattractive processing step for Level II assemblers.

In the description by Baldwin & Higgins, a laminated organic PWB is stencil printed with solder paste. The corresponding flip-chips are dipped in a low solids (i.e., "no clean") flux, and placed onto the solder paste pads. For all operations, machinery with highly accurate alignment technology is required. The flux is designed to be tacky, so the components will stick to the solder paste. The assembly is then placed in a belt-furnace, where it is heated to the reflow temperature using a controlled temperature profile. After reflow, the ICs are underfilled using an epoxy that is filled with silica to tailor the thermal expansion to a value inbetween the Si IC (~3 ppm/°C) and an FR4 board (~18 ppm/°C). Underfilling is achieved by applying a liquid-cure epoxy at one or more edges of the IC and allowing capillary forces to draw it between the IC and board. In all cases, a fillet is desired (like a bead of caulking) along the outside edge of the IC in order to maximize the shear strength and keep foreign materials out.

Under-Bump Metallurgy (UBM) for Pb-Free Integrated Circuits

Solders are used to join IC's to the substrate and the substrate to the PWB. However, in all cases there exists one or more intermediate layers that provide a

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[4] See previous footnote and [Gileo 2002]. The authors report that unpackaged IC's can be difficult to test fully. A partial test will not eliminate all the defective IC's from the assembly line. Consider an example where an assembly is made from a single board with 3 board-mounted IC's. If only one IC is defective, then the entire assembly becomes defective. Since FCOB assemblies normally cannot be reworked, the board and the two functioning IC's must be scrapped. As the number of IC's per board rises, so does the chance of a defective assembly.

solderable surface and keep the solder from reacting with other components. On the IC (or die) side, this is commonly referred to as under bump metallurgy (UBM). An excellent paper on Pb-free solder reliability is given by K. Zeng and K. Tu [Zeng & Tu 2002] where six case studies are reviewed. This work will be revisited in the next chapter.

[Jang & Paik 2001] consider the interaction of four different UBM's with Sn-Ag solder. These are listed in the Table 2-1, below. All materials are sputtered, except where noted.

Table 2-1 – Summary of Pb-Free UBM's Used in [Jang & Paik 2001]

No.	Base Layer	Layer 2	Layer 3	Solder
1	TiW	Cu	Electroplated Cu	Sn-3.5%Ag and eutectic Sn-Pb
2	Cr	Cr-Cu	Cu	
3	NiV	Cu		
4	TiW	NiV		

Each UBM system must meet a challenging list of requirements. The authors state that important parameters include the ability to deposit low-stress films (for reliability), compatibility with selective etching (for electrodeposition lithography), a chemistry that is well understood (for reliability), good performance as a diffusion barrier, low contact resistance and finally low cost. All requirements are met to some extent, although there are complications. A summary of the pros and cons of each system, as detailed by Jang and Paik is given below.

UBM No. 1 is reportedly the most popular for Pb-Sn or Pb-free applications. It relies on a thick Cu layer to form Cu-Sn IMCs. The TiW layer serves as a good diffusion barrier for Cu. There are two major problems with this system. First, the Cu-Sn IMCs can be thick enough to crack. Second, stresses can build up that cause cratering of the IC.

The Sn-3.5%Ag solder was observed to be compatible with UMB No.1, although the Cu-Sn IMCs were thicker than with Sn-Pb.

UBM No. 2 is based on the original IBM C4 process. The Cr serves as an excellent diffusion layer, but does not wet Sn. The Cr-Cu layer is meant to serve as a buffer between the two elements. If all the Cu is consumed by IMC formation, the solder will no longer be able to bond to the pad.

UBM No. 3 uses Ni as a Sn-wetable diffusion boundary that works by forming a Sn-Ni IMC. The V is added in order to increase sputtering efficiency. This system was reportedly developed by Delco Electronics.

UBM No. 4 is a hybrid of 1 and 3. As before, the TiW serves as a diffusion barrier and the Ni in the NiV forms an IMC that slows the advance of Sn. Jang and Paik state that this system was developed by Toshiba.

All UBM systems seem to be compatible with Sn-3.5%Ag, although each has its failure mechanisms and none are perfect.

Pb-Free Printed Wiring Board (PWB) Finishes

Aside from solders, Pb seems to enjoy widespread use in electronic components. An important field of research is removal of Pb from PWB finishes. As will be seen in this section, a finish must satisfy a number of requirements, and there are many metallurgical issues to contend with.

[Wu et al 2004] have investigated the growth of intermetallic compounds (IMC's) during thermal cycling. In this case, an unfinished Cu-leaded IC package is soldered to a finished Cu PWB pad using a Pb-free, Sn-3wt%Ag-0.5wt%Cu (SAC) alloy. The Cu IC lead is bent outward in the shape of a "J" and is thus called a small-outline J (SOJ) lead. Two PWB pad finishes are used in separate experiments, and the growth of IMC layers is compared. The first finish is an electroless Ni layer over the Cu pad, plus an immersion-plated Au layer over top the Ni. According to Wu et al, the Ni is used as a diffusion barrier between the

Cu PWB pad and the Sn in the solder. The Au layer protects against Ni oxidation, which would inhibit solderability. The second finish is called an organic surface preservative (OSP).

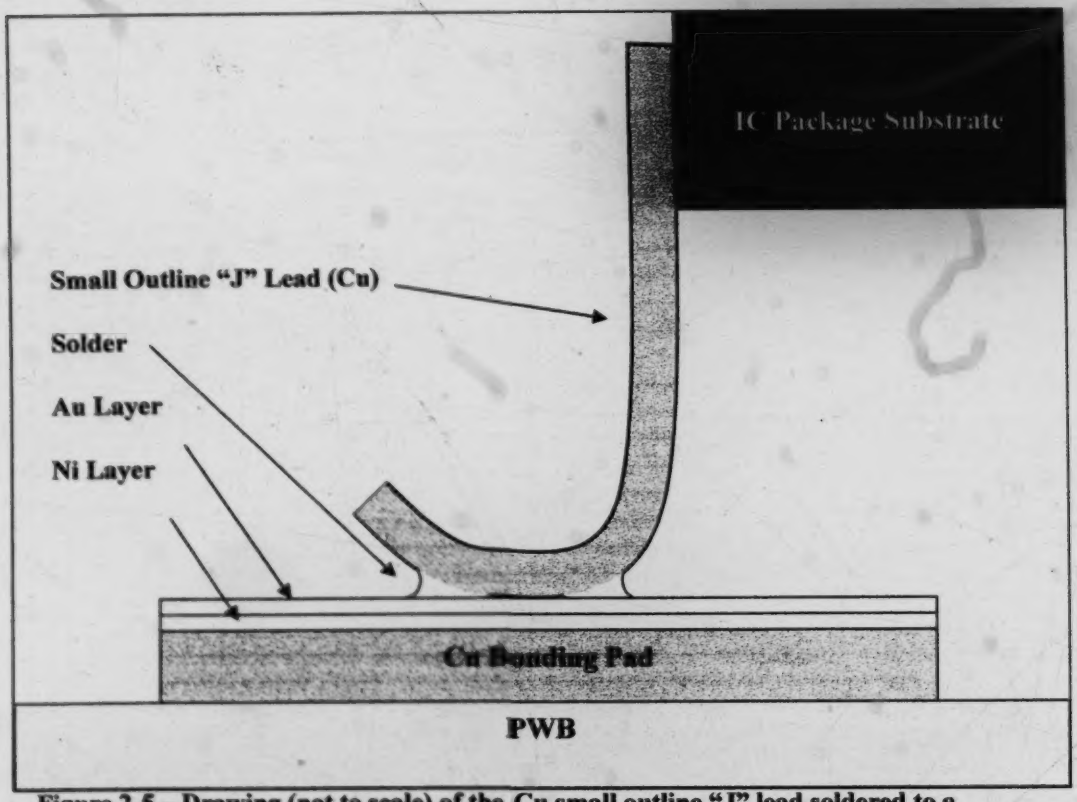

Figure 2-5 – Drawing (not to scale) of the Cu small outline "J" lead soldered to a PWB finish as reported by Wu et al in Figure 1 of their work. Drawing by Olsen.

Note that diffusion barriers are even more important for Pb-free solders, which contain substantially more Sn than eutectic Sn-Pb and are therefore much more reactive with Cu substrates. [Humpston & Jacobson 2004].

The thermal cycles were reportedly between -40°C and +125°C with a high-temperature dwell time of 15min and a 5min heating and cooling ramp. The samples were then polished, and the growth of IMC layers between the Cu SOJ lead and SAC solder were analyzed via microscopy. The results were found to vary with surface finish. For example, the presence of Ni affected the thickness and composition of the IMC layer, but not the growth kinetics. Note that the Ni

was originally present on the PWB pad, as shown in Figure 2-5, but some of the Ni had diffused into the entire solder bulk. With Ni/Au, only Cu_6Sn_5 is present for at least 1000 cycles and the IMC is thinner than the OSP sample. If OSP is used, the IMC is thicker and it contains both Cu_6Sn_5 (near the SOJ lead) and Cu_3Sn (near the solder). The Cu_3Sn appeared after about 500 thermal cycles.

In an effort to rationalize their findings, Wu et al assume that the small amount of Au, and Ag from the solder, will always exist as intermetallics with Sn. This reduces the system to a Sn(Au-Ag)-Cu-Ni pseudo-ternary. They point out the presence of a thermodynamically stable region of Sn(Au-Ag)-Cu_6Sn_5-Ni_3Sn_4 near the Sn-rich side of the solder bond. It is then reasoned that Sn(Au-Ag)-Cu_3Sn-Ni_3Sn_4 (which contains more Cu) cannot exist. Finally, the ternary phase diagram used was plotted for 240°C, and they assume it is also generally valid for 125°C.

It would seem plausible, however, that Cu_3Sn could grow on the Cu SOJ surface. Other references [Lee & Duh 1999][5] point to preferential formation of Cu_6Sn_5 on a Sn-rich solder/Cu pad interface at the time of soldering with the formation of Cu_3Sn during aging at elevated temperatures. This situation could describe Wu et al's experiment with the OSP, where a Sn(Ag)-Cu pseudo-binary alloy exists. Nevertheless, Wu et al's study seems to suggest that the Ni inhibits growth of Cu_3Sn at temperatures up to 125°C. Further, both papers report IMC growth that is proportional to the square root of time.

The thickness, distribution and composition of IMC's at the solder-component and solder-PWB pad interfaces are important, because they influence joint strength, thermo-fatigue and fracture performance of the solder bond [Yanagawa et al 2004]. In fact, IMC's and other foreign phase particles have been purposely added to form solder composites with enhanced properties. These phases include

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[5] [Lee and Duh 1999] offer a number of other references on this topic. They use a Sn-Cu solder with small amounts of Al and <0.02mol% Ni.

nanometer- to micrometer-sized Cu_6Sn_5, Cu_3Sn, Ni-Ti shape memory particles, TiO_2 and Al_2O_3 [Wang et al 2002], [Dutta et al 2004].

As mentioned previously, the other method of protecting and enhancing the solderability of Cu pads on a PWB is through a process called Hot Air Solder Leveling (HASL, or HAL). Pb-free alternatives to eutectic Sn-Pb have been developed. According to [Lawrence &. Eichhorst 2004], two of the most popular Pb-free PWB pad finishes are based on Sn-Ag and Sn-Cu that contain rare (expensive) elements and are prone to corrosion or undesirable metallurgical reactions.

For Sn-Ag and Sn-Cu, trace amounts of organic additives and other metals are also added. Both systems are reported to be more difficult to process than eutectic Sn-Pb, and special care must be taken to ensure temperature homogeneity. The above authors do not favour Sn-Ag, due to the cost of Ag and its tendency to oxidize and migrate through Cu and Sn. Lawrence works for a company called Pentaplex, which has licensed the use of a patented[6] Sn-Cu eutectic solder that contains trace Ni. Provided that temperature fluctuations are minimized, the HASL finish performs well.

A fairly comprehensive review of PWB finishes is given by [Hwang 2005], wherein HASL and other alternatives are discussed in detail. According to Hwang, HASL finishes are the most solderable. Unfortunately, they are also increasingly unable to yield a finish whose flatness and thickness is good enough to allow the bonding of components with ever-shrinking features. HASL is also tough on thermally-sensitive components.

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[6] Lawrence and Eichhorst report that this Sn-Cu eutectic composition is patented by Nihon Superior. The wave-soldering version of this alloy is called SN100C, and the HASL version is SN100CL.

All the alternatives reported by Hwang tend to be less solderable and more costly than HASL, but solve the aforementioned problems. These are listed below:

- Electroless Pd/Cu
- Immersion Pd/Cu
- Immersion Au/electroless Pd/Cu
- Immersion Au/electroless Ni/Cu
- Electroplated Au/Electroplated Ni
- Immersion Au/Electroplated Ni
- Electroplated Au/Electroless Ni
- Immersion Bi
- Immersion Sn
- Immersion Ag
- Organic Solderability Preservative (OSP, benzotriazole)

According to Baldwin & Higgins, electroless plating involves no application of current. Rather, a metal salt is reduced on a prepared surface using a chemical reducing agent. The main advantage is the absence of applied current. This means that electrically isolated, conductive surfaces or even nonconductive surfaces can be coated. The process can be difficult to control, however, and the rate of deposition is generally an order-of-magnitude lower than electrolytic methods. The process is discussed further in Chapter 3.

Immersion plating is a different process. Hwang describes this as a redox process wherein a sacrificial layer of metal is oxidized into ion form, while another element is reduced from ion to metal. According to Hwang, immersion plating only occurs on the surface, and is therefore suitable for very thin films only. However, one would expect that the film would be as continuous and flat as the sacrificial film.

Each system is described by Hwang, but of special interest to this thesis is immersion Sn. The Sn (from $SnSO_4$ or $SnCl_2$) is deposited on Cu, some of which is oxidized in order to reduce the Sn at ~65°C. The deposit is an IMC, and the film is flat and economical. Drawbacks include the inability to use wire bonding and poor performance in certain applications. As a final note, Hwang reports that while the OSP is cheap and easy to inspect, it has a number of drawbacks that include extended reaction of Cu with the solder, and poor oxidation resistance above 95°C.

Developments with Pb-free Solders

Unlike Pb-based solders, there is a seemingly endless list of Pb-free alternatives under consideration. The main driver for the elimination of Pb from all electronic components is legislation in Japan and the EU [Pb-Free 2005], [Turbini et al 2001], [Bastow 2003], [Rae 2002], [Fukuda et al 2003], [Subramanian & Lee 2003], [Suganuma 2001], [Suraski & Seeling 2001].

Despite the legislative push, there are compelling reasons against the adoption of Pb-free electronics. As an example, Turbini et al provide arguments supporting the continued use of Pb-based solders. They argue from an industrial ecology perspective that considers studies from the Environmental Protection Agency (EPA) in the US on Pb pollution from landfill sites and incinerators. In both cases, the impact of Pb seems to be very low. Of greater concern is the fact that the most promising Pb-free solders must be processed at higher temperatures, which drives energy consumption upwards. The environmental impact of Ag is also poor, as it tends to leach into groundwater at unacceptable levels. Finally, the amount of Pb in typical electronic products is small. For example, a laptop computer only contains about 10g [Suganuma 2001].

On the other hand, Turbini et al do recognize a need for better recycling of Pb in electronics since the EPA has documented that Pb can leach into groundwater. This problem is underscored by the relatively large growth rate in electronics production, and the limited number of adequate recycling facilities. Overall, there

is a strong public perception that Pb is harmful to human health and the environment. Over the last 50 years or so it has also been a favorite target for (successful) reduction efforts by society at large [Lasky & Morvan 2002]. This may explain the passing of legislation in Japan and the EU. A number of large companies such as Alliance Semiconductor [Alliance 2004] are following suit and now offer a substantial array of products.

As mentioned in Chapter 1, there are other good reasons to switch to Pb-free, however. Solders, such as Sn-4%Ag, are superior to eutectic Sn-Pb in many ways. For example, Sn-4%Ag has lower electrical resistivity, better thermal conductivity and better physical properties than Pb-Sn solder [Humpston & Jacobson 2004].

As mentioned above, a popular PWB bond pad finish is Au/Ni/Cu. [Zeng and Tu 2002] consider the interaction of Sn-Pb and Pb-free solders with this finish. They state that a problem with Au/Ni/Cu PWB bond pad finish is the dissolution of Au in Sn-Pb solders. After the Sn dissolves the Au layer, it attacks the Ni to form Ni_3Sn_4. The formation of this intermetallic is desirable, since it serves as a good diffusion barrier and is preferable to the faster growing Cu-Sn intermetallics. However, the dissolved Au forms $(An,Ni)Sn_4$ intermetallics within the solder that redeposit on the Ni_3Sn_4 to form a weak IMC layer that degrades shear strength and thermal fatigue resistance.

Oddly enough, Zeng and Tu state that these reactions do not occur with Pb-free solders, even though the Sn content is higher. They attribute this to the possibility that Pb changes the interfacial energy of the solder enough to encourage ripening of the undesirable phases.

On the other hand, the authors also illustrate a case where an SAC solder is used to join a Au/Ni(P)/Al PWB bond pad directly to an IC with Al/Ni(V)/Cu UBM. This would be a chip on board (COB) packaging technique. The result is IMC spalling on the IC side. If the PWB bond pad is pure Cu, then no spalling occurs.

As with previous Level I examples, one can conclude that Pb-free solders come complete with their own materials issues that must be carefully sorted out before widespread adoption can take place [Turbini et al 2001].

While most of the references used in this paper tend to report the reliability of Pb-free replacements with caution and then prescribe more research, it should be noted that there are many examples of corporate adoption of Pb-free solders. A good reference of activity in the Japanese electronics industry is given by [Fukuda et al 2003].

In practice, Pb-free solders tend to contain mostly Sn. As mentioned in Level I, Sn has much more of a tendency than Pb to form IMC's that can be detrimental to solder performance. Further, Sn has an infuriating tendency to form whiskers. This issue is addressed below.

Solder-Free Level II Connections

[Onodera et al 2004] have considered a method of producing very fine pitch interconnects on an IC package substrate using a modified Au wire bonding technique. Their approach is to wire ball bond an IC to a metal substrate, which is then covered with epoxy encapsulant. Later, the package is flipped over and the substrate etched away to reveal the bottom surface substrate ball bonds. A single ball-bond is formed on these exposed Au surfaces, and the package is glued to a board.

Pb-Free Level II Component Finishes

Traditionally, PWB contacts were finished with a film of Sn-Pb solder. The solder was applied and then reflowed into a coherent film using a technique called Hot Air Solder Leveling, or HASL. While other Pb-free formulations are reportedly being developed, [Swanson and Zhang 2002] state that other non-HASL finishes are becoming more popular. These include immersion Ag, Au or Sn, and even organic finishes.

While Pb-free solders will be covered later, Swanson and Zhang note that the most popular Sn-Pb replacement is Sn-Ag-Cu, or SAC. However, there are aforementioned concerns regarding the environmental impact of Ag [Turbini et al 2001], [Pb-Free 2005]. It is important to note that all Pb-free PWB and component finishes should be compatible with Sn-Pb and SAC.

All soldered components are conductive metals. Component leads (such as those illustrated in Figure 1-8 around the QFP), must be coated with a protective finish that resists corrosion and enhances solderability. Popular finishes are Sn-(0.7-1.5%)Cu, Sn-(≤3.5%)Bi, Sn-(3.5%)Ag and pure Sn. Each is compatible with Sn-Pb and SAC, but all suffer from whiskering, in addition to other attributes, which are discussed below.

According to Swanson and Zhang, Sn-Cu was probably the first system to be investigated by researchers, who thought that the presence of Cu would suppress whiskering. This wisdom is questioned by the authors, who feel instead that Cu may enhance whiskering.[7] They show an SEM photo of a whisker that has been sectioned using a Focused Ion Beam (FIB). At its base is a Sn-Cu intermetallic phase. As will be seen in the next section, the whiskering phenomenon is complex, and may be attributable to other characteristics of the film. Finally, Sn-Cu electroplating solutions suffer from two forms of degradation. The first is accelerated oxidation of Sn(II) to Sn(IV) due to the presence of Cu. The second is undesirable immersion plating, wherein Cu ions will dissolve Sn metal and deposit as Cu metal without the application of current.

Like Pb, Bi seems to reduce the whiskering problem. This is one reason for its appeal and a Pb-replacement candidate. Probably the biggest drawback, however,

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[7] While this may be a problem, it should be noted that Sn-Cu has been successfully used as a solder [Snowdon et al 2000]. The main issue is storage of as-plated films, rather than reflowed Sn-Cu, as mentioned by Lal et al.

is the fact that Bi will form a very low melting-point eutectic with small amounts of Pb. This will therefore be an issue for any company that handles Pb along with Pb-free. Like Sn-Cu, Sn-Bi plating solutions also are reported to suffer from immersion plating.

Sn-Ag is the final alloy candidate mentioned by Swanson and Zhang. Aside from environmental concerns, Sn-Ag is reportedly a very difficult system to plate. The authors feel that a lot of work (ca. 2001-02) still needs to be done before Sn-Ag (and even Sn-Cu or Sn-Bi) can be considered a reliable commercial alternative to Sn-Pb.

Pure Sn is also mentioned as a component finish. Surprisingly, it is considered by the authors as probably the best alternative to Sn-Pb. Reasons include simplicity in plating, especially compositional control (since there is only one element) and compatibility with a wide range of electronic applications. This conclusion is still debatable, however, as discussed in Chapter 4.

Chapter 3: Thin Film Deposition

Introduction

The purpose of this chapter is to give a brief introduction to some of the popular technologies for producing thin films on substrates. The two main approaches to metal film deposition are physical (vacuum) based and (wet) chemistry based, and each deposition method is described accordingly. The major emphasis in this thesis is electrodeposition, and as such it will receive the most comprehensive review.

In many cases, accurate mathematical modeling of thin film deposition processes is a difficult problem. As will be seen, direct current (DC) plating and pulsed current (PC) plating processes are no exception [e.g., Bard & Faulkner 2001]. In addition, the models rely on empirical or system-specific data. Detailed modeling and measurements are beyond the scope of this thesis. However, a number of general trends will be discussed.

Film Deposition Methods

Overview

The following review is based on [Barlow et al. 1997]. Physical deposition techniques include evaporation, sputtering and variations of the two. Chemical deposition techniques include chemical vapour, electroless plating and electroplating. The electroplating summary in the next section is based on other references, as noted below.

Physical (Vacuum) Deposition Techniques

Physical deposition is a vacuum-based technology that involves the formation of structures using an extremely low background pressure. The strength of vacuum

can vary between ~10^{-1} Pa (10^{-3} torr[1]) and 10^{-10} Pa (10^{-12} torr), depending on the technique used and the desired film properties. The two main techniques that will be described here are evaporation and sputter deposition.

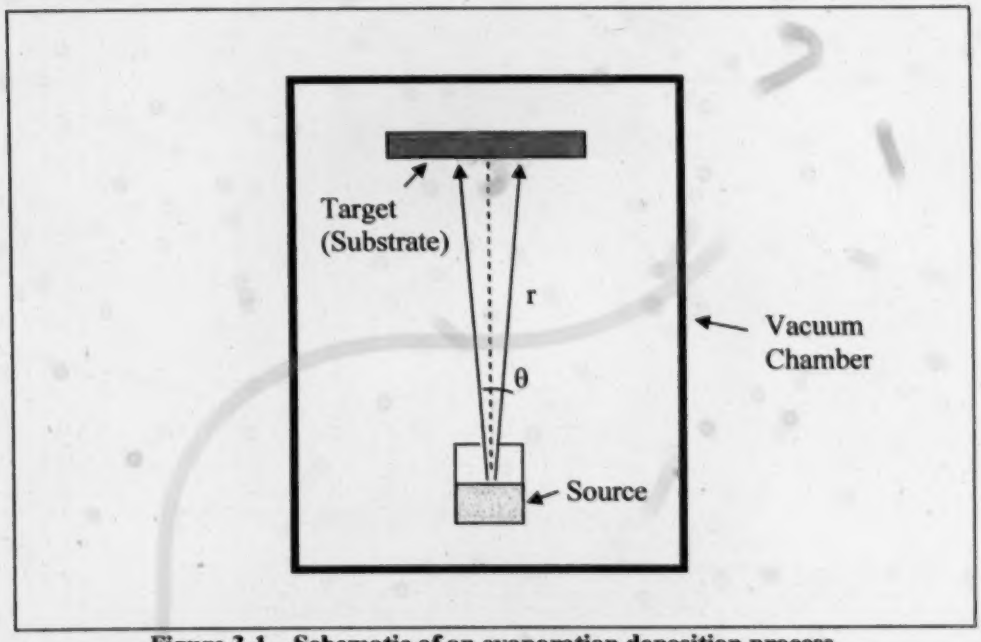

Figure 3-1 – Schematic of an evaporation deposition process.

Evaporation

The simplest vacuum deposition technique is evaporation which occurs by melting or sublimating a sold material within a heated container called a boat. Films are deposited on a substrate. Both the boat and substrate are placed in an evacuated chamber. The vapour that is produced from a melted or sublimated material will condense on the substrate to form a growing film. Deposit properties are controlled mainly by varying the substrate temperature, as this will affect the mobility of adatoms on the film surface. A schematic is shown in Figure 3-1.

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[1] 1 torr = 1 mm Hg = 133 Pa

The use of a vacuum is critical for a number of reasons. First, oxidation of the source, vapour and deposit is greatly reduced. Second, the mean free path of the vapour atoms is increased to the point where a regular flux of material from source to substrate is achieved. The rate of deposition is dependent upon a number of variables. These are incorporated into the Hertz-Knudsen equation shown below,

$$\frac{\partial N}{\partial t}\frac{1}{A} = \frac{\alpha(p''-p)}{\sqrt{2\pi mkT}} \qquad (3\text{-}1)$$

where:

$(\partial N/\partial t)(1/A)$ = deposition rate from the source with area A

α = coefficient of evaporation (higher with cleaner source surface)

m = molecular weight of the substance being evaporated

k = Boltzmann's constant

T = temperature

p" = vapour pressure at evaporant surface

p = hydrostatic pressure on the surface of the source

With the above equation, it is necessary to rely on tabulated values such as α, which may be expected to change for an evaporation source depending on the type of use, the laboratory environment and even among vendors.

The rate of deposition is highly directional. In other words, one should expect to obtain line-of-sight coverage that will vary with substrate geometry. In fact, the deposited film shown in Figure 3-1 will be thicker at the center than at the edges. This deposition rate variation can be described using the Knudsen cosine law, according to $\cos\theta/r^2$.

Evaporation can be a straight-forward technique. Possibly its major advantage is the avoidance of wet chemistry so one only requires a pure material, instead of a

dissolved metal salt. A wide variety of materials can be deposited in this manner, by varying the way in which the source is heated.

Alloy films can be grown by melting two or more materials together or in separate boats, and this was done by IBM to produce high Pb alloys for Level I bumping (C4 process) [Gileo 2002]. Alloying can be a difficult venture, however, since the vapour pressures of each element must be carefully controlled in order to attain good compositional control in the deposit. Finally, the substrate can be made from a wide range of materials, and it does not need to be conductive.

For metals with high vapour pressure, deposition can be fairly rapid. Unfortunately, Sn is not one such metal. While it melts at a relatively low 232°C, its boiling point is rather high at 2337°C. Therefore, the temperature required to obtain a 10^{-6} Pa vapour pressure is about 1000°C (vs. ~600°C for Pb).

Further drawbacks include the use of vacuum pumps and evacuated chambers. It can take hours to obtain the proper vacuum before a film can be deposited, and at least part of the vacuum chamber must be opened to air after completing a batch of product. Some materials are highly reactive in their molten or gaseous state, which raises safety and deposit purity issues as well. Liquids can react with the sample boat, while vapours can react with contaminants in the chamber. Typically, the adatoms have a low bonding energy (~0.5eV), and this can result in films with poor adhesion to the substrate. In comparison, sputtered films are bonded with kinetic energies between 10 and 100eV.

There are a number of variations on the evaporation process, including novel ways of heating the sample without risking chemical reactions with the boat. These include the use of a guided electron beam to heat a small area of sample. Molecular beam epitaxy is another variation of evaporation. It is an ultra-high vacuum technique that employs pressures as low as 10^{-10} Pa (10^{-12} torr). It exhibits low deposition rates, but can deposit materials one crystal layer at a time,

and in a way that closely matches the crystal structure of the substrate. This is especially useful for applications such as doped GaAs semiconductor lasers [e.g., Lau & Mayer 1990].

Sputtering[2]

Sputtering involves the erosion of a material (called a "target") into small particles using plasma. These particles are carried along a stream of plasma onto a substrate, where they are deposited. The plasma is typically made from Ar gas, which is slowly introduced into the chamber and ionized under the influence of a large electric field. Initially the chamber pressure is about 10^{-5} Pa (10^{-7} torr). After a constant flow of Ar gas is introduced, the pressure drops to about 10^{-1} Pa (10^{-3} torr).

Sputtering offers many advantages over evaporation. To begin, the source material (target) is not melted or sublimed. There is therefore less concern about reactions with the sample holder. Secondly, multiple materials can be deposited by including multiple targets. As with evaporation, the substrate can be made of any material (conductive or otherwise). Thirdly, high melting point materials like refractory metals are easily sputtered. Finally, sputtering imparts a great deal more energy to the substrate, which often translates to better adhesion.

Variations on the sputtering technique include more efficient mechanisms for creating plasmas (e.g., use of a "magnetron"). Older sputtering systems used a dc field, which caused problems when depositing nonconductive materials. Newer innovations incorporate alternating electric fields, which reduce detrimental charge buildup on nonconductive substrates. They can also be used to deposit smoother films by reverse-sputtering features with high relief. In many ways, DC and AC sputtering are analogous to DC and reverse-pulse electroplating.

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[2] In addition to the above-mentioned sources, this summary is based on the author's personal experience depositing sputtered metallic thin films.

Sputtering is a popular thin film deposition method because it is compatible with a wide range of materials. This is possibly its biggest advantage, especially since such materials can be deposited using essentially the same procedures. In addition, the material to be deposited remains in solid-state form; there are few if any precursor or processing chemicals that are required, including strong acids or bases, hazardous solvents, or waste materials that are difficult to treat. In contrast, electroplating requires separate solutions for each metal or alloy. Further, chemical waste issues abound, and it would be difficult to develop a single machine that could easily plate a wide variety of materials.

Aside from flexibility, sputtering has a number of other attractive features. As mentioned previously, sputtered films are deposited using a large amount of kinetic energy, meaning they are normally well adhered to the substrate. In addition, deposition under vacuum helps to ensure a low amount of contamination during deposition (although one should expect to require wet chemical cleaning steps for surface preparation). Finally, several high purity films of different composition can be deposited sequentially in a single vessel without fear of cross-contamination.

Drawbacks exist as well. They include the use of a vacuum and very slow deposition rates when compared to electroplating.

Chemical Deposition Methods

In contrast to physical deposition, chemical deposition methods tend to offer faster rates of deposition. In addition, Barlow et al note that chemical vapour deposition (CVD) is possibly the most versatile film deposition technique, owing to the large number of materials and available processing options. The three major chemical deposition techniques are sol gel, CVD and plating.

Sol Gel

Sol gels start as chemical solutions that are applied using a variety of procedures. These include dipping or spin casting, and cause a chemical mixture known as a

sol to be coated over the substrate. After applying the film, the mixture is destabilized so that it turns into a gel. Afterwards, the gel can be further processed into a final form. For example, metal oxide films can be processed from a metal alkoxide precursor sol and converted to a gel with water (i.e., via hydrolysis). The water is carefully removed and the gel is then fired at high temperature to create a fully dense ceramic film. Overall, the chemistry involved is quite complex, and one would expect the systems to exhibit sensitivity to fluctuations in temperature or humidity during manufacturing, storage and use.

Chemical Vapour Deposition (CVD)

[Barlow et al. 1997] present a generic CVD procedure. First, gaseous reactants move from a storage cylinder to the reaction chamber. Second, the reactants are activated by heating or energizing with plasma. The activated reactants are now called precursors. Next, the precursors move over heated substrates in order to react or condense as a film. As a result of the condensation reactions, a film begins to grow. Reaction products from the growth are expelled from the substrate surface and carried away by the flow of gas.

A summary of the main types of CVD process is given in Table 3-1. Drawbacks of all CVD processes include the relatively toxic and corrosive nature of the byproducts in the waste gas. These must be carefully handled and "scrubbed" before releasing to the environment.

Table 3-1 – Summary of CVD processes (from descriptions in [Barlow et al. 1997])

Process	Typical Products	Notes
Metalorganic CVD	III-V and II-VI semiconductor films	Reactants are organometallic and energized with heat
Plasma-Enhanced CVD	Diamond, silicide, Si, refractory metal films	Reactants are energized with plasma
Atmospheric Pressure CVD	Oxide, silicate glass films	No vacuum requirement. Best suited to continuous processing

Electroless Plating

Plating describes two technologies: electroplating and electroless plating. During electroplating, an applied electric field is used to deposit a film by means of chemical reduction on a conductive substrate. During electroless plating, a similar reduction occurs, although it does not require either an applied field or conductive substrate to occur. Electroplating is described in much more detail in the following section, while electroless plating will be summarized here. According to [Barlow et al. 1997], electroplated films are used for a variety of electronic applications. These include interconnect metallizations, Au and Ni pads for wire bonding and more recently, bumps for flip chip and TAB.

For electroless applications, the authors describe processes for Cu, Ni and Au. They state that electroless deposition is best suited for "soft" substrates that have enough surface roughness or porosity to ensure good bonding. They cite PWB bonding pads and plated through holes (PTH's) as examples. On the other hand, flat ceramic substrates with a dense grain structure are not ideal and must be further prepared. Below is a summary of the method for electroless deposition of Ni-P.

Before Ni and P can be deposited, the surface must be sensitized. Barlow et al. describe the use of $Pd[SnCl^{3-}]_n$ salt, which is hydrolyzed to form Pd metal + $Sn(OH)_2$ + $Sn(OH)_4$. The Pd is deposited on the substrate surface and acts as a seed layer for Ni + P deposition from a bath containing Ni-hypophosphite. Deposition follows two reactions:

$$Ni^{2+} + H_2PO_2^- + H_2O \rightarrow Ni + H_2PO_3^- + 2H^+ \qquad (3\text{-}2)$$

and

$$H_2 + H_2PO_2^- \rightarrow P + 2H_2O \qquad (3\text{-}3)$$

The P content in the film is controlled by adjusting the pH of the bath. Concentrations of P are normally between 2 and 12%, and greatly affect the final properties of the Ni-P film. A typical bath pH is reported to be 4.5.

Some of the advantages of electroless plating have been described previously. These include the ability to plate on electrically isolated or nonconductive substrates. In addition, the process is good at depositing films on complex geometries, and the lack of an applied electric field means that deposition is more uniform in thickness.

Electrodeposition Theory

Direct Current Plating

Overview

The following summary is based on the work of [Bard & Faulkner 2001], [Lee 1999] and [Popov et al 2002].

Electrodeposition (or electroplating) involves the chemical reduction of ions in solution by means of an applied electric current. Many chemical reactions are homogeneous because they occur almost anywhere within a defined volume. Electrodeposition is different; it is a heterogeneous process because it occurs over specific locations on a surface. Such surfaces are called electrodes, and they must be in contact with two separate media in order to function. The first is a solid-state conductor, such as a Cu wire while the second is an electrolyte. Current flows through the wire by electron migration and through the electrolyte by ionic transport.

Figure 3-2 illustrates a basic electrochemical cell. In its current configuration, current will flow spontaneously through the wire. On the left side a single reaction occurs:

$$Zn \rightarrow Zn^{2+} + 2e^- \qquad (3\text{-}4)$$

This is known as an oxidation reaction, since electrons are lost. An electrode that supports oxidation is called the anode, although its polarity is dependent upon the properties of the entire cell. On the right side, the following reaction occurs:

$$Cu^{2+} + 2e^- \rightarrow Cu \qquad (3\text{-}5)$$

This is known as a reduction reaction, since electrons are gained (although the amount of positive charge is reduced). An electrode that supports reduction is called the cathode. The combination of an oxidation and reduction reaction is called a redox reaction. Note that in both reactions there is a change between aqueous and solid state, though this is not necessary for a redox reaction to occur. In addition, redox reactions are not only found in electrochemical cells; corrosion is a redox reaction that occurs without capturing any useful energy.

Each redox reaction is given a potential that must be overcome before it will proceed to the left or right. A common way of representing the barrier is by listing each reaction as a reduction, and measuring the minimum voltage against a normal hydrogen electrode. When an oxidation reaction occurs, it is written as a reduction whose voltage is given an opposite sign. The overall potential of the cell is simply the difference between the two. Assuming 1 M concentrations at 298 K (i.e., standard conditions), one may use standard reduction potentials found in text books. This is shown for the example in Figure 3-2.

Reaction		Standard Reduction Potential, ε^0 (V vs. NHE)[3]
Anode:	$-(Zn \rightarrow Zn^{2+} + 2e^-)$	-(-0.7626 V)
Cathode:	$Cu \rightarrow Cu^{2+} + 2e^-$	+0.340 V
Overall:	$Zn + Cu^{2+} + 2e^- \rightarrow Cu + Zn^{2+} + 2e^-$	+1.103 V

[3] The values for reduction potentials and all constants within this section are taken from [Bard & Faulkner 2001].

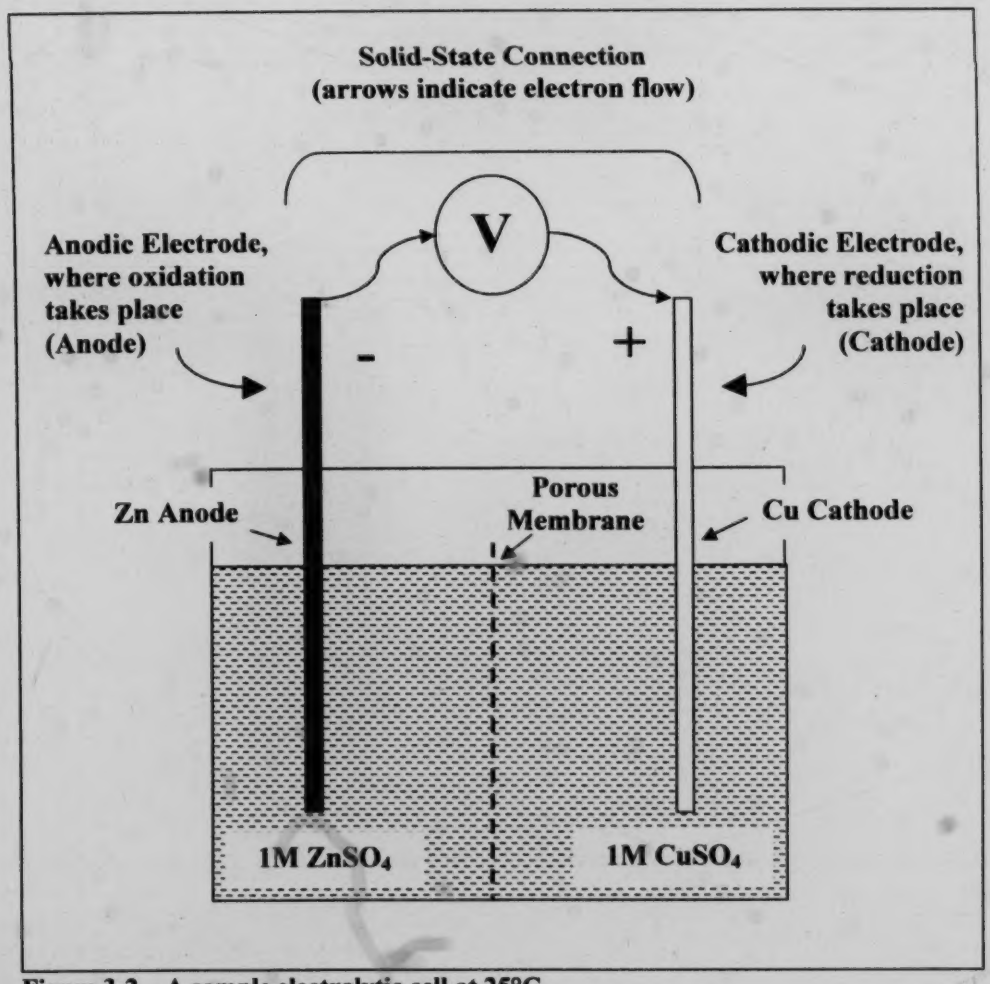

Figure 3-2 – A sample electrolytic cell at 25°C.

The above example describes an electrochemical battery, where Zn is dissolved at the anode and Cu is plated at the cathode. Because the overall cell potential is positive, the reaction will proceed from left to right. However, it is possible to slow, stop and even reverse the process so that Zn is plated and Cu dissolved. This is done by applying a voltage over the wire with opposite polarity. As the applied voltage approaches -1.103 V, the amount of current flow will be reduced. At -1.103 V, no current will flow and the system is at equilibrium. Beyond -1.103 V the process works in reverse and by convention the polarity is switched.

Electroplating cells work in the same way; a minimum voltage is supplied to an electrochemical system in order to initiate and support a reduction reaction.

However, the reduced species is normally a metal, and it must be reduced to a neutral (solid) oxidation state in order to obtain a deposition product.

An example of an electroplating cell is given in Figure 3-3. Here a single electrolyte composition is used, and the anode is made from an inert material. Note that for any reduction reaction there must also be an oxidation reaction. In addition, more than one reaction can occur when more than one species is present.

In Figure 3-3 there are two Pt electrodes and an aqueous electrolytic solution of 1M H_2SO_4 plus 1M $SnSO_4$. Before any redox reactions take place the compounds must dissolve in the water and the following reactions are expected to occur:

$$H_2SO_4 \rightarrow H^+ + HSO_4^- \qquad (3\text{-}6)$$

$$HSO_4^- \rightarrow H^+ + SO_4^{2-} \qquad (3\text{-}7)$$

$$SnSO_4 \rightarrow Sn^{2+} + SO_4^{2-} \qquad (3\text{-}8)$$

From the literature [Lee 1999], one can determine the extent to which each reaction will proceed based on the equilibrium constant. Reaction (3-6) will go to completion, since H_2SO_4 is a strong acid. Reaction (3-7) does not carry fully to completion, and for this example it will be assumed that the dissociation does not occur at all. As such, the concentration of H^+ (denoted $[H^+]$) is equal to 1M. For reaction (3-8), $SnSO_4$ is highly soluble and therefore $[Sn^{2+}]$ also equals 1M.

A list of possible reactions and standard reduction potentials (ε^0) is given below. Note that oxidation occurs at the anode and the possible reactions are written as such, even though a reduction potential is given.

Possible Anode Reaction	ε^0 (V vs. NHE)	
$2\ SO_4^{2-} \rightarrow S_2O_8^{2-} + 2e^-$	+2.010 V	(3-9)
$2H_2O \rightarrow O_2 + 4H^+ + 4e^-$	+1.229 V	(3-10)

$Pt \rightarrow Pt^{2+} + 2e^-$	+1.188 V	(3-11)

Possible Cathode Reaction	ε^0 (V vs. NHE)	
$O_2 + 4H^+ + 4e^- \rightarrow 2H_2O$	+1.229 V	(3-12)
$2H^+ + 2e^- \rightarrow H_2$	0.0000 V	(3-13)
$Sn^{2+} + 2e \leftrightarrow Sn$	-0.1375 V	(3-14)
$SO_4^{2-} + 2H^+ + 2e^- \rightarrow SO_3^{2-} + H_2O$	-0.221 V	(3-15)

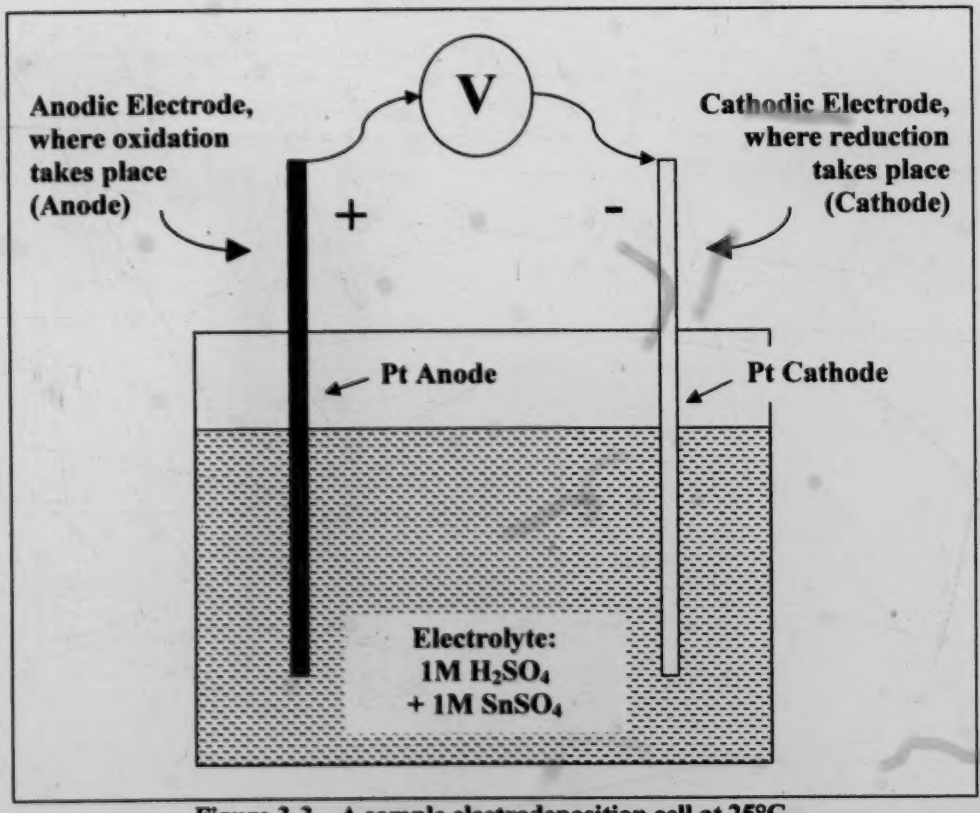

Figure 3-3 – A sample electrodeposition cell at 25°C.

The rule is that the reaction with the least positive reduction potential will most likely occur on the anode, and the reaction with the most positive reduction

potential will most likely occur on the cathode. Under the condition of an applied voltage, the thermodynamically predicted reactions are:

$$\text{Anode: } Pt \rightarrow Pt^{2+} + 2e^- \qquad (3\text{-}16)$$

$$\text{Cathode: } O_2 + 4H^+ + 4e^- \rightarrow 2H_2O \qquad (3\text{-}17)$$

In reality, these preferential reactions may not take place due to kinetic effects. In fact, Pt is highly resistant to oxidation and so the reaction is very slow. This means that the next reaction $2H_2O \rightarrow O_2 + 4H^+ + 4e^-$ is more likely to occur. On the cathode, if the plating bath does not contain dissolved O_2 then (3-17) cannot occur. Therefore the potential will change so that the next reaction $2H^+ + 2e^- \rightarrow H_2$ will probably proceed. If instead Sn is to be plated, the setup must be modified so that the reduction of Sn^{2+} is more likely to occur than H. Two possible methods include reducing the H^+ concentration and exchanging the Pt cathode with a material that exhibits a large hydrogen reduction overpotential. Each method is discussed below.

The Nernst Equation and Concentration Effects

As mentioned, the listed reduction potentials apply for chemical species under standard conditions (1 M and 298 K). If either parameter is changed, then the reduction potentials can also be expected to change. A theoretical relationship describing the change in reduction potential is called the Nernst Equation, shown below. Note, however, that it is derived under the assumption of chemical reversibility, meaning that the relation may not apply under all conditions.

For the reaction:

$$aA + bB \rightarrow mM + nN$$

where A, B, M and N are reacting species (elements or compounds)

a, b, m and n are stoichiometric coefficents

we have

$$E = E^0 - \frac{RT}{nF}\ln\left(\frac{a_M^m a_N^n}{a_A^a a_B^b}\right) \qquad (3\text{-}18)$$

Here E^0 is the standard reduction potential (all species at 1M and 298 K)

E is the adjusted reduction potential

R is molar gas constant: 8.31447 J/(mol*K)

T is the temperature in Kelvins

n is the number of electrons transferred in the redox reaction

F is Faraday's constant: 96485.3 C/mole of electrons

a is the species activity

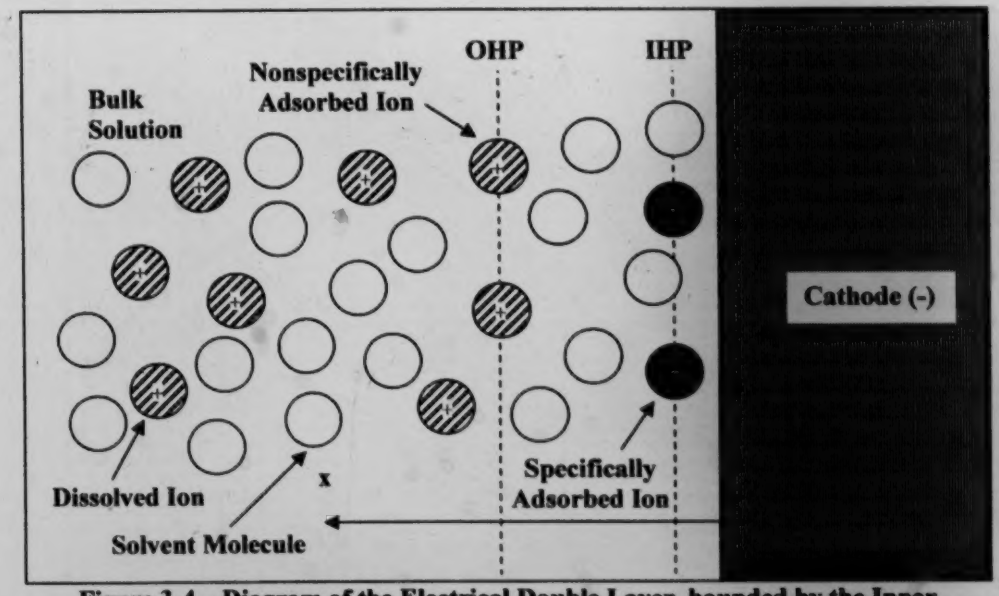

Figure 3-4 – Diagram of the Electrical Double Layer, bounded by the Inner Hemholtz Plane (IHP) and the Outer Helmholtz Plane (OHP). The IHP contains ions that are "specifically adsorbed," and therefore are able to be very close to the cathode surface. The OHP is the closest point to the cathode that the bulk (specifically unadsorbed) ions can reach. The distance between the IHP and the OHP is the double layer, and it acts as a capacitor that absorbs charge.

In the case of H^+ reduction, one has $2H^+ + 2e^- = H^2$ with a standard reduction potential equal to a normal hydrogen electrode, or 0.000V. Using the Nernst equation yields the following:

$$E = 0.000V - \frac{8.31447\frac{J}{mol \cdot K} \cdot 298K}{2 \cdot 96485.3C} \ln\left(\frac{1}{[H^+]}\right) \qquad (3\text{-}18a)$$

The shift in potential is cathodic (i.e., more negative) although its magnitude is small. Going from 1M H^+ down to 0.1M yields a shift of only -0.06V. Note that variations in Sn^{2+} concentration will also change the reduction potential.

A second way to make Sn^{2+} reduction more likely is to replace the Pt cathode with another material that exhibits a high overpotential for H^+ reduction. In addition to thermodynamic potential, the rate at which two protons can bond to form H_2 gas is highly dependent upon the supporting surface. Slow kinetics can induce a significant cathodic overpotential.

Kinetics and Boundary Layer Effects

As previously mentioned, electrodeposition occurs at an interface between the electrolyte and solid-state conductors. The interface is a cathodic surface, though the reactions it supports are complex and not fully understood. However, it is possible to summarize some relevant occurrences here.

To begin, electrodeposition occurs on a cathode which by convention is given a negative polarity. During deposition, positive ions (cations) are drawn from the bulk of the electrolyte to a layer just above the electrolytic interface by electrostatic forces and random diffusion. The layer is defined by the inner and outer Helmholtz planes (IHP and OHP), although Bard & Faulkner note that the IHP is also called the compact, Helmholtz or Stern layer. At the IHP, ions are present as "specifically adsorbed" species that are capable of being reduced. The OHP represents the closest point that regular or "nonspecifically adsorbed" ions can approach the cathode. The region between the IHP and OHP is known as the

electrical double layer, and this is important for electrodeposition because the double layer acts as a very thin capacitor that must be charged in order for reduction to occur. Double layer charging is known as a nonfaradaic process, while reduction is a Faradaic process. In some cases nonfaradaic processes can consume a large amount of current, meaning that less current is available for reduction.

During the electrodeposition work in this thesis, a fixed average current density was maintained until a predetermined amount of charge was transferred. Under such conditions, a constant level of applied current is generated by the power supply. According to Bard & Faulkner, the result is a dynamic voltage requirement that is described by the following equation:

$$\varepsilon = i\left(R_s + \frac{t}{C_d}\right) \tag{3-19}$$

where ε = required potential in volts

i = applied current

R_s = resistance of the solution, or plating bath

t = time

C_d = capacitance of the double layer

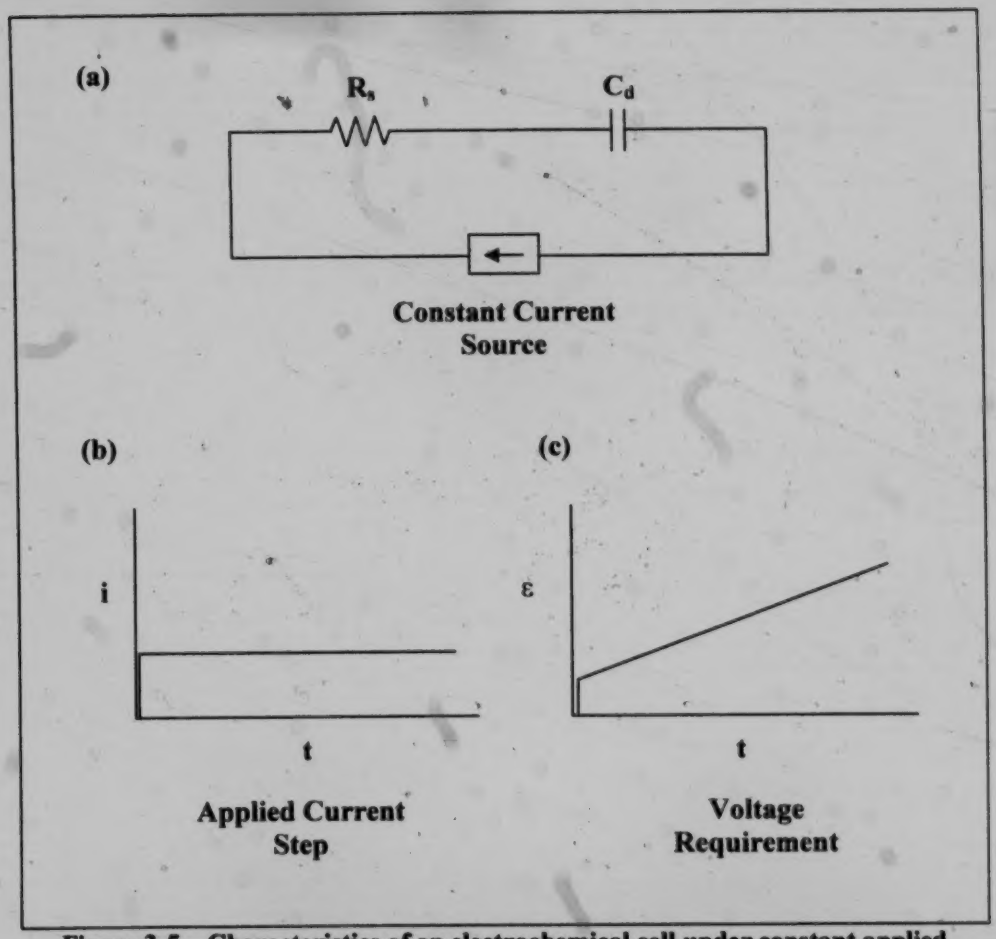

Figure 3-5 – Characteristics of an electrochemical cell under constant applied current. Drawing based on Figures 1.2.8 and 1.2.9 of [Bard & Faulkner 2001].

Equation (3-19) is based on the well-known E = i*R relation, where potential is the product of current and resistance. In this case, cell resistance is the sum of solution resistance and the need to charge the double layer. A schematic of the equivalent circuit for an electroplating cell, the applied current and resulting voltage requirement is given in Figure 3-5 (a) to (c).

Note that the voltage buildup is predicted to continually increase. If the current is supplied in pulses, however, the double layer will repeatedly charge during application of current and discharge when no current is applied. This phenomenon serves to introduce a system lag, and is considered in the next section.

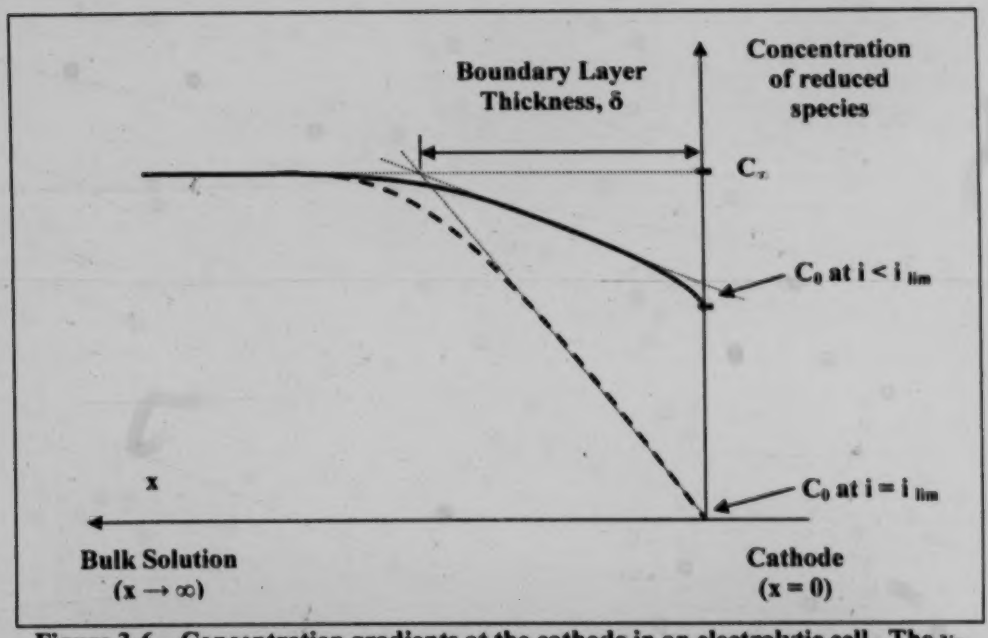

Figure 3-6 – Concentration gradients at the cathode in an electrolytic cell. The y-axis is kept on the right to maintain a "cathode-on-the-right" convention adopted in this thesis. The boundary layer thickness (δ) is an estimation of the ion-depletion zone, based on the slope of the concentration (C) versus distance curve. C_∞ is the concentration of ions in the bulk of the solution. C_0 is the concentration of ions at the cathode (where x=0). Note that C_0 is equal to zero when the applied current (i) is equal to the limiting current (i_{lim}).

Ultimately, electrodeposition occurs as a result of Faradaic processes such as electrolytic reduction of ionic species at the cathode. However, at zero cell potential the concentration of ions is assumed to be constant throughout the electroplating solution. As an electrolytic potential is applied, the ions near the cathode are reduced to solid form and the local concentration drops. The result is the buildup of a concentration gradient as illustrated in Figure 3-6. Normally the concentration gradient is modeled as a linear function whose slope is dependent upon the rate of ionic reduction, or Faradaic current transfer. In electrolytic systems that are sufficiently large,[4] the ionic concentration of the bulk solution can be considered as constant. As the rate of reduction increases, the concentration gradient will become steeper until ions are being reduced as fast as

[4] In this case, large enough so that the bulk ion concentration, C_∞, remains unchanged.

they are transported to the cathode. This situation is called the limiting current density (j_{lim}), and occurs when the effective concentration of ions at the cathode surface is zero (C_0=0). From the concentration slopes shown in Figure 3-6, it is possible to quantify the distance between the cathode and a point where the ionic concentration is essentially equal to that in the bulk solution. This is called the boundary layer thickness (δ).

The above discussion is important to electroplating, because it illustrates the kinetic nature of electrochemistry while forming a link between current and potential. Note that the reduction potential can be increased further and this will enable a second species to be reduced. Such a method is used to plate alloys from a single solution.

Pulsed Current (PC) Plating

Overview [Puippe 1986-1]

Pulse plating involves the modulation of current or voltage, and many different waveforms can be employed. A few examples are shown in Figure 3-7. Like DC plating a cathodic voltage is applied to generate a corresponding average current output. Unlike DC, a pulsed waveform exhibits at least one peak current density that is not equal to the average current density. A basic square wave pulse is shown in Figure 3-7(a). It is a repeating step function that alternates between a peak current density ($j = j_{pk}$) and zero current ($j = 0$) over two specific time intervals. For such a waveform it is possible to quantify the relative on/off times according to the following equation:

$$p(\%) = \frac{t_{on}}{t_{on} + t_{off}} * 100 \qquad (3\text{-}20)$$

Where p is the pulse duty (specified in percent),

t_{on} is the time at $j = j_{pk}$

t_{off} is the time at $j = 0$

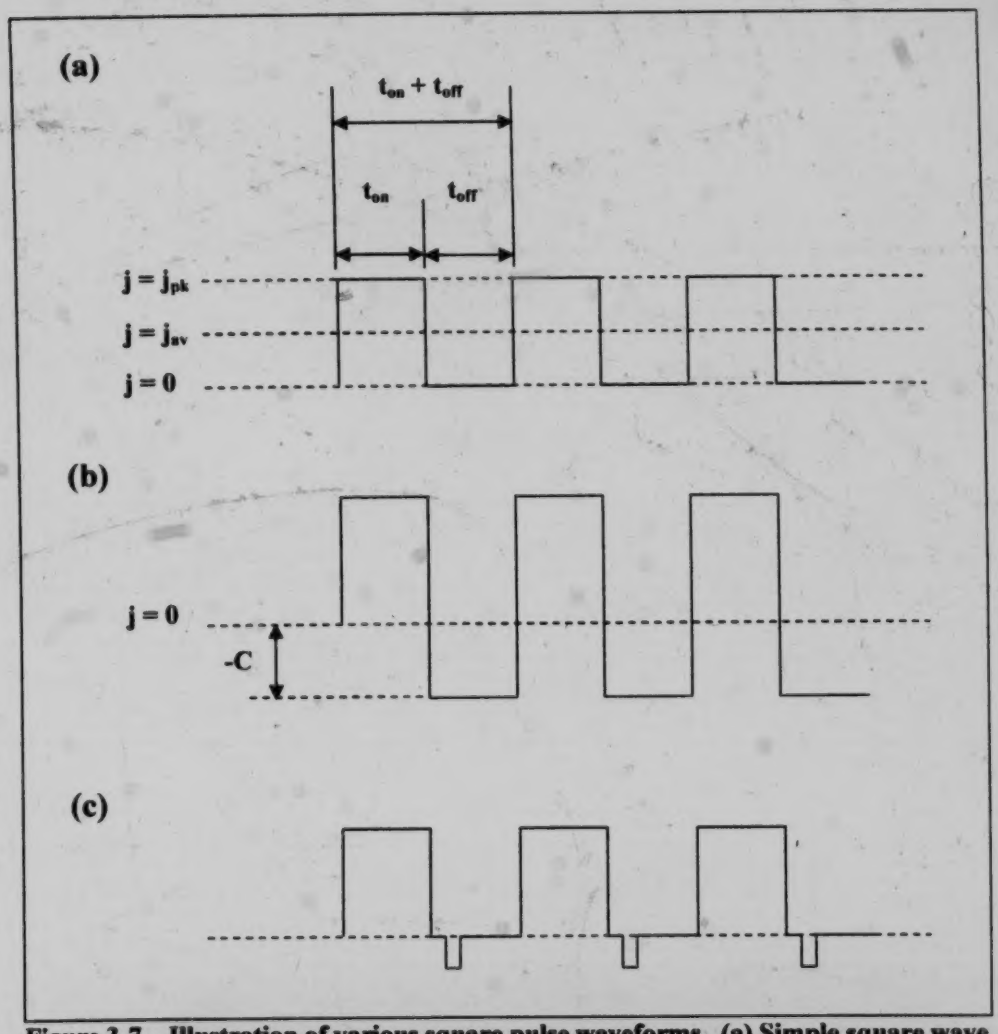

Figure 3-7 – Illustration of various square pulse waveforms. (a) Simple square wave pulse used for experimental work in this thesis, (b) shifted square wave pulse, to allow reverse pulse plating, (c) simple square wave pulse with a short reverse pulse, used for experimental work in this thesis.

The same description applies to the waveform in Figure 3-7(b), although it is displaced by a constant (-C). Note that there is no time at which the current is zero. Figure 3-7(c) is similar to (a), except that there is a small reverse pulse originating from zero current. This waveform is expected to cause an electrochemical system to behave differently from (b), since there is a fair amount of time spent with no applied current (i.e., at rest). Puippe notes that an electrodeposited film can be very dynamic at rest because it allows adsorption, desorption and recrystallization processes to occur. When p=100%, the pulsed

waveform becomes a horizontal line, which is simply DC plating. A much more comprehensive list of waveform variations is given in [Puippe 1986-1].

For the waveform in Figure 3-7(a), average and peak current densities are related by the following equation:

$$j_{pk} = \frac{j_{avg}}{p} \tag{3-21}$$

Note that in all cases $j_{pk} \geq j_{avg}$, and they are equal only for DC plating (p=100%).

The use of different waveforms can allow for great flexibility over DC plating, although there are always electrochemical limitations that must be considered. For example, the capacitor-like double-layer is formed at the cathode-electrolyte interface, which collects charge during t_{on} and releases charge during t_{off}. The second limitation has to do with mass transport from the bulk of the electrolyte to the cathode.

The rate of charging (and discharging) is dependent upon not only the current density, but also the electrolyte. Regardless of its value, Puippe stresses the importance of applying pulses that are at least 10 times longer than the amount of time required to charge and discharge the double layer. If this is not done, the actual pulses that are experienced by the electrochemical system are distorted. The distortions serve to minimize the benefits of pulsing, such as modification of film structure, and one is left basically with DC plating. This will be considered in more detail at the end of the chapter.

PC plating shares many common traits with DC. For example, the concentration of metal cations near the cathode is depleted as they are reduced to a neutral metal deposit. New cations are replenished as a result of migration, diffusion and convection, and the concentration profile is often assumed to be linear. In PC plating, Puippe describes a second phenomenon that occurs. During a current pulse the concentration profile is reduced more quickly at the cathode than for an

equivalent DC current. This is because as one moves from DC plating, the magnitude of a cyclic pulse must always be larger if the same average current is to be transferred. The result is a narrower, but steeper concentration gradient near the cathode, shown in Figure 3-8. This is due to the fact that $j_{pk} > j_{avg}$, and the fact that each pulse is relatively fast.

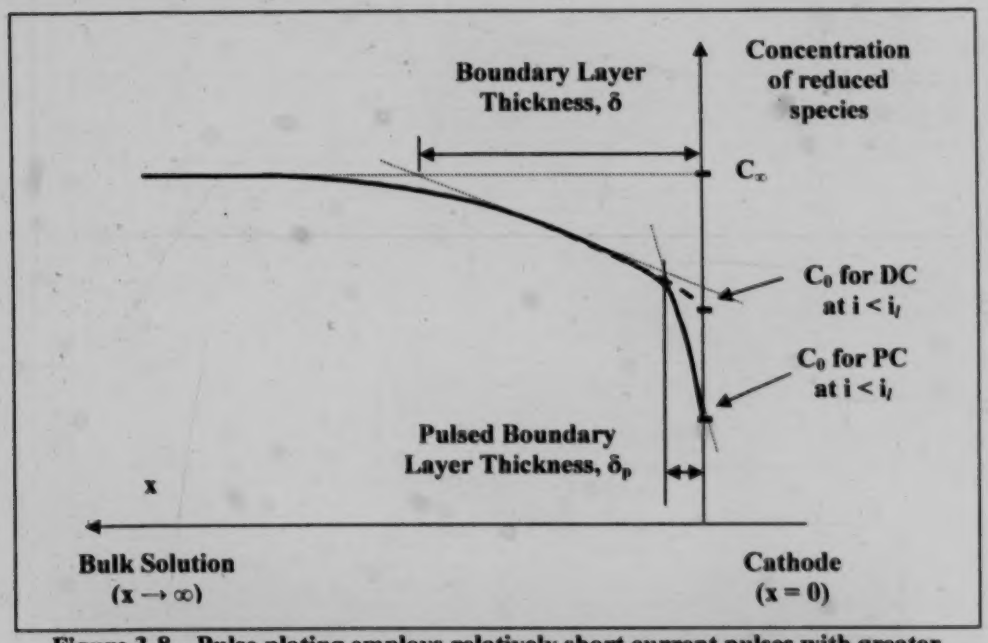
Boundary Layer Thickness, δ
Concentration of reduced species
C_∞
C_0 for DC at $i < i_l$
C_0 for PC at $i < i_l$
Pulsed Boundary Layer Thickness, δ_p
x
Bulk Solution ($x \rightarrow \infty$)
Cathode ($x = 0$)

Figure 3-8 – Pulse plating employs relatively short current pulses with greater magnitude than the average current density. [Puippe 1986-1] claims that this changes the concentration gradient near the cathode.

From this new concentration profile arises the mass-transfer limitation. Puippe has determined from [Landolt 1986] that there exists a maximum useful pulse duration, called the transition time. Below the transition time, current efficiency is maintained, meaning that most or all of the desired reaction will occur. Low current efficiency arises when other, undesirable reduction reactions consume current. Note that j_{avg} is always less than the limiting current density (j_l) that is realized during DC plating. Puippe stresses this second fact in order to debunk claims in the literature which state that j_{avg} for pulse deposition can exceed j_l for DC plating. Other researchers have shown that "practical" current densities have been exceeded using PC plating, but this advantage is marginal over DC plating.

In this context, it is assumed that "practical" means a j_{avg} value that reliably yields good deposits.

After describing the limitations, Puippe considers the benefits of PC plating. The first is the ability to influence nucleation and growth tendencies of a deposit. The second is its influence on kinetics.

Nucleation of new crystals and growth of existing ones are seen as competing processes. They are encouraged by the following conditions:

Nucleation	Growth
- High adatom concentration	- Low adatom concentration
- Small surface diffusion rates	- Large surface diffusion rates
- High overpotentials	- Low overpotentials

During PC deposition, one has the option of prescribing a high j_{pk} with p approaching zero percent to encourage nucleation, or low j_{pk} with duty approaching unity (DC) to encourage growth. Results are often seen by the apparent grain size, where nucleation-encouraged deposits exhibit finer grains.

Puippe sees proportionality between overpotential and adatom concentration. By raising overpotential, more adatoms will be drawn to the electrode surface, thereby raising the local concentration. Surface diffusivity is another matter; while he states that the adsorption isotherm of adatoms is a function of potential, diffusivity itself is highly influenced by the presence of other adsorbed species, such as organic additives. That said, one can expect a pulsed current to continuously change the presence or behaviour of adsorbed species, which is not the case in DC.

According to this description, deposits will increase in mass due to incorporation of new crystals and/or growth of existing ones. During the off-times of a PC, the deposit may still be rearranging its structure via recrystallization. The strength of this mechanism, however, is dependent upon the material to be deposited [Puippe 1986-2].

Finally, Puippe reports the possibility of plating with high j_{pk} values that make the adatom concentration too high to allow for crystalline nucleation or growth to occur. In this case, the deposit will be amorphous.

The second benefit to PC is control over kinetics. Normally, one might find secondary (or undesired) processes (such as hydrogen evolution) to become dominant at certain plating potentials. However, if the kinetics of a secondary process could be suppressed, then the primary (desired) process might continue to dominate. Therefore, deposition rates of the desired element during t_{on} can be much larger than DC deposition at j_{avg}.

Another example of controlled kinetics is during alloying plating. Here the composition of a deposit can be changed by changing PC conditions. Puippe illustrates the effect in Figure 3-9, below. By changing the potential from a to b, the rate constant (k) of reaction 1 (Me I) increases more than that of reaction 2 (Me II). One would therefore expect an increase in Me I content at b as compared to a.

Puippe notes, however, that adsorption and desorption rates of competing species can be affected by changing t_{on} and t_{off} values. As such, one may find critical time values wherein expected trends are no longer followed.

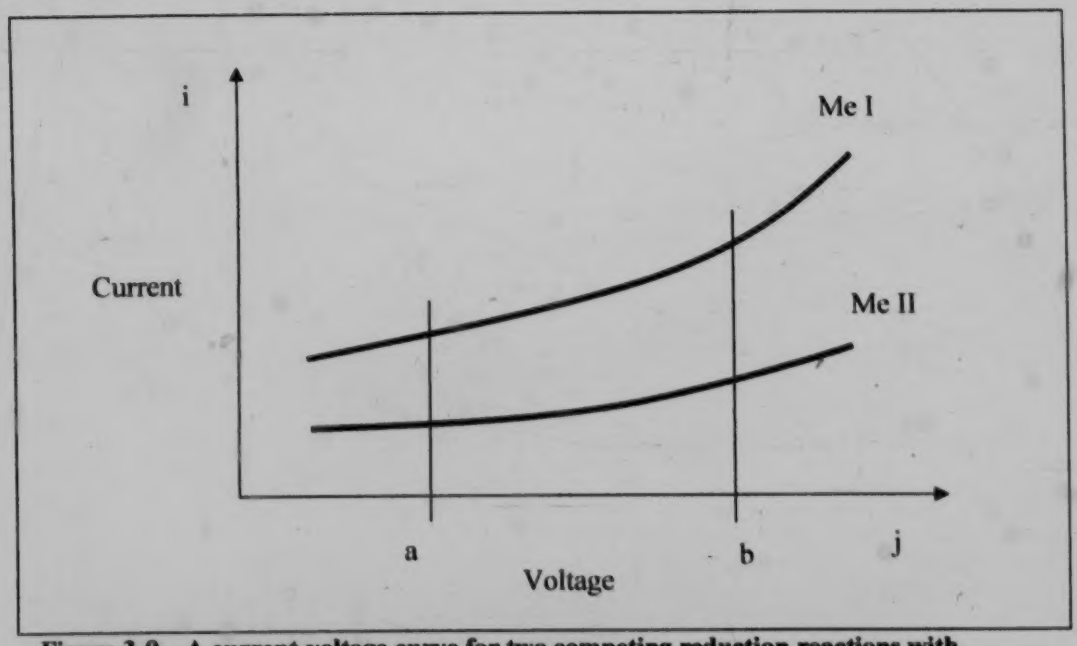

Figure 3-9 – A current-voltage curve for two competing reduction reactions with different kinetics. Me I = Reaction 1, Me II = Reaction 2. (Redrawn from Puippe, p.7)

Puippe further states that there are two main methods of PC plating. The first is current-controlled and the second is voltage-controlled. While each has pros and cons, this thesis is concerned only with the second. Within each PC method, there are a variety of ways in which the pulses can be controlled. Puippe gives special mention to reverse-pulsing, noting that it is particularly useful for producing smooth films with consistent thickness.

A drawback of basic PC plating is the effect of decreasing activation overpotential with increasing j. This leads to less equalized current distribution, meaning more current (and therefore more deposition) at peaks and less in the valleys. However, pulse reversing can help mitigate this problem by using the unequalized current distribution to preferentially dissolve the peaks.

Finally, it is possible to use much more complex PC waveforms as a way to maximize the benefits of both cathodic (depositing) and anodic (dissolving) pulses. This is done by employing more complex (e.g., nested) waveforms.

Electrochemical Kinetics in Pulse Plating [Cheh 1986]

PC plating has two effects on kinetics. The first has to do with Faradaic current, which is a function of continuous charging and discharging of the electrical double layer. The second effect on kinetics is a function of cyclic changes in metal ion concentrations.

Within an electrochemical system, the total applied current density (j) is composed of Faradaic (j_f) and nonfaradaic (j_n) current densities:

$$j = j_n + j_f \tag{3-22}$$

Note that j_n is what charges the electrical double layer, while j_f powers the reduction of cations to form a metal deposit. Cheh further defines j_n as a "transient process" in terms of electrical double layer capacitance (C_d), electrode surface potential (η_s), and time (t).

$$j_n = C_d \, d\eta_s/dt \tag{3-23}$$

To contrast, note that $j_n = 0$ for DC plating. In a sense, the double layer becomes a "current dashpot" that forms near the cathode surface. It diverts charge that could support electrodeposition during t_{on} and later supports the electrodeposition process by discharging during t_{off}.

Cheh describes a hypothetical example taken from Wan et al[5] of $Cu^{2+}+e^- \rightarrow Cu^+$ (reaction 1 at j_1) and $Cu^+ + e^- \rightarrow Cu$ reduction (reaction 2 at j_2). Each reaction competes with the other, and their respective fractions of j_f are calculated. In this example, current efficiency represents the fraction of j_f consumed by $Cu^+ + e^- \rightarrow Cu$. The theory is of limited application, however, since the current densities for each

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[5] C.C. Wan, H.Y. Cheh and H.B. Linford; Journal Chinese Institute of Chemical Engineers, 9: 69 (1978), cited by Wan et al but not reviewed within this thesis.

reaction over specific intervals of the pulse must be known and these are difficult values to determine.

The example supposes that reaction 1 is dominant for the first 0.1s of a 1.0s pulse cycle, but reaction 2 still proceeds at a known current density. Next, reaction 2 becomes dominant during the second 0.1s due to lowered concentration of Cu^{2+} at the cathode. It proceeds at a known current density, and for the remaining 0.8s both reactions proceed at an equivalent and known current density. The total charge consumed by reaction 2 divided by the total charge supplied by the Faradaic current is the Cu plating efficiency.

The point of Cheh's example is that the surface concentration of the metal(s) to be deposited will affect both the rate of deposition (reduction) and deposit structure. If reduction to a neutral species occurs in a single step, then overpotential varies with time as a pulse is applied. If more than one step is required, Cheh has experimentally determined that PC plating favours the first step only, meaning that the plating efficiency is lowered. However, quantitative descriptions become complex, since one requires knowledge of the relationship between process rates and surface concentrations arising from mass transfer.

Crystallization [Puippe 1986-2]

During electrodeposition, mass transfer occurs via migration, convection and diffusion. When ions cross the double layer, crystallization can occur. Two mutually competitive crystallization processes are nucleation and growth, and both have a direct impact on deposit morphology and porosity. Fortunately, the relationship between pulse plating parameters, morphology and porosity tend to be easily quantified. Other deposit properties that are dependent upon pulse parameters include crystallographic orientation, the presence of phases (including additives and hydrogen gas) and even lack of crystallinity, though these are harder to quantify.

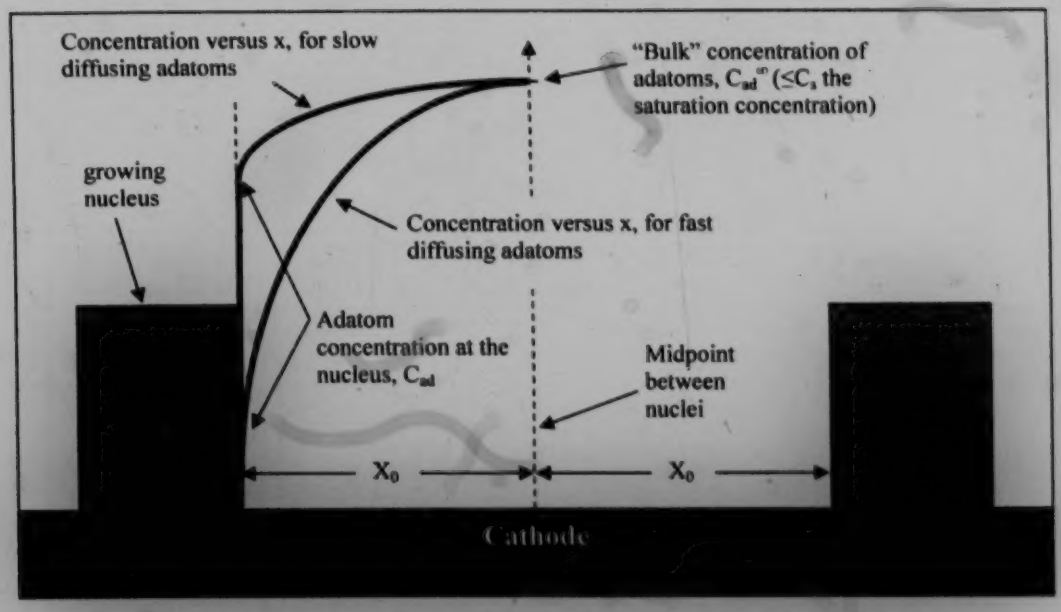
Concentration versus x, for slow diffusing adatoms
"Bulk" concentration of adatoms, C_{ad}^{∞} ($\leq C_s$ the saturation concentration)
growing nucleus
Concentration versus x, for fast diffusing adatoms
Adatom concentration at the nucleus, C_{ad}
Midpoint between nuclei
X_0
X_0
Cathode

Figure 3-10 – Diagram showing concentration profiles of fast- and slow-diffusing adatoms at various locations. This drawing is based on descriptions and Fig. 3.1 of [Puippe 1986-2].

After charge transfer has occurred on the cathode, ions become adatoms and it is reasonable to assume that they will appear at random spots along the cathode. If nuclei exist on the surface, adatoms at these nuclei will contribute to their growth and be depleted. The resulting concentration gradient will encourage diffusion of adatoms from regions devoid of nuclei to regions that have nuclei. Puippe sets up a model, as shown in Figure 3-10, and describes the crystallization (growth) potential as follows:

$$\eta_k = \frac{RT}{nF} \ln \frac{C_{ad}^{\infty}}{C_{ad}} \qquad (3\text{-}24)$$

He states the following relationships:

- High C_{ad} values drive lower crystallization overpotential (η_k)
- Fast-diffusing adatoms have a lower crystallization overpotential
- Slow-diffusing adatoms have a higher crystallization overpotential

If η_k gets too large, new nuclei will form according to equation (3-25):

$$\nu = k_1 \exp\left(\frac{-k_2}{|\eta_k|}\right) \qquad (3\text{-}25)$$

where ν is the nucleation rate

k_1 is a constant

k_2 is proportional to the energy required for 2D nucleation

From this, Puippe draws the following conclusions:

- The nucleation rate increases exponentially with increasing overpotential
- New nuclei decrease x_o, since their number per unit area increases
- As x_o decreases, C^{∞}_{ad} will also decrease
- Decreasing C^{∞}_{ad} causes a decrease in η_k (equation (3-24))

Note that Equations (3-24) and (3-25) illustrate mechanisms to achieve a balance between nucleation and growth, although this balance is system-dependent.

Other parameters can be used to influence adatom mobility, such as the exchange current density, i_0. However, overpotential is most easily modified. Puippe describes a system where i_0 and mobility are held constant. Pulse plating becomes an optimal approach to varying overpotential, which in turn affects the balance of nucleation and growth in equations (3-24) and (3-25). By increasing overpotential (over smaller time increments), one encourages nucleation (and smaller grain size) over growth, and vice versa.

Puippe also considers the effect of current density (j), off time (t_{off}) and on time (t_{on}) on deposit morphology. He stresses that the observations made are at $j/j_{lim} << 1$, where j_{lim} is the limiting current density. In this way, mass transfer effects are negligible.

The effects of PC current density on morphology can be examined using at least two methods. The first is by maintaining constant pulse *duration* and j_{avg} while increasing j_{pk}. The second is by maintaining constant pulse *charge* and j_{avg} while increasing j_{pk}.

Puippe uses method 1 to observe trends in Cu, Cd and Pd deposits. For both Cu and Pd, finer structures are seen with higher pulsed j. With Cd, the opposite occurs. The reason has to do with the need to increase the off time in order to increase j. Some systems (such as Cd) change their structure during off time, so the trend observed with Cu and Pd is masked.

The second method is devised to get around this problem. During any given pulse, the amount of charge (corresponding to the number of atoms deposited) is kept constant. As a result, lower j pulses have longer on-times than higher j pulses. The effect is to keep t_{off} more constant than in method 1. Puippe states that lower j pulses will supply the same number of atoms, but at a lower energy than the high j pulse. By using method 2, the Cd films behave just like Cu and Pd, showing finer structures with higher overpotentials.

For certain systems, t_{off} can be a time period with lots of crystallization activity. Sometimes small features will be plated, but if enough time is allotted between pulses these will recrystallize into larger features. Use of the second method can be a good way to observe these trends.

Puippe discusses a Cd deposit from $CdSO_4$ solution, whose surface activity seems to be modified by the species in solution (possibly SO_4^{2-}) during off times. Longer "off" times may cause more extensive changes. In another system, Cu exhibits finer features at somewhat longer t_{off} times, but at significantly longer off times, features become much larger.

The effects of t_{on} are system dependent. Puippe looks at the $Cd^{2+} + SO_4^{2-}$ system and finds that longer t_{on} times tend to increase the size of Cd deposits. He concludes that larger Cd features form since extended t_{on} times allow growth to

progress, while t_{off} times allow deposition of species that inhibit growth and enhance nucleation.

Puippe also considers the effects of PC plating on film porosity and growth. He states that given the enhanced nucleation of a pulsed current, one should expect to see less transverse (plan view) porosity. Higher nucleation rates encourage intergranular growth, which also reduces pores.

Finally, it should be noted that a major source of film inclusions is entrained organic additives. From experience, Puippe states that PC-plating deposits tend to exhibit smaller amounts of additives from both organic and inorganic sources. Gasses such as hydrogen, oxygen and nitrogen can follow similar trends, for reasons stated above.

Double Layer Charge and Discharge [Puippe 1986-3]

For a square wave pulse with t_{off} at zero current, there is charging of a system during t_{on} and discharging during t_{off}. This is because of a capacitive effect within the system. If the current density (mA/cm^2) supplied is j_P which is equal to the total current, j_t, then:

$$j_P = j_C + j_F = j_t \qquad (3\text{-}26)$$

Where j_C is the capacitive current (which charges the double layer) and j_F is the Faradaic current (which powers the redox reactions).

During t_{on}, j_C will decrease and j_F will increase until it equals j_t or the pulse stops. The time it takes for j_F to reach j_t is called the charging time. Short charging times mean that the electrochemical system will experience a pulsed waveform that is similar to the one that is generated. A long charging time ends up skewing this waveform. The same principle is applied during t_{off}, when the double layer is discharged. In either case, if the charging time is longer than t_{on}, or if the discharging time is longer than t_{off}, then the current will never reach the maximum or minimum value specified by the waveform generator.

If one assumes a charge transfer-limited reaction (i.e., no mass transfer effects):

$$j_F = j_0\left(\exp\frac{\alpha n F \eta_a}{RT} - \exp\frac{-(1-\alpha) n F \eta_a}{RT}\right) \qquad (3\text{-}27)$$

which is the Butler-Volmer equation, where

j_F = Faradaic current

j_0 = exchange current density

α = transfer coefficient, which is a measure of oxidation vs. reduction barrier symmetry [Bard & Faulkner 2001]

n = number of electrons transferred

F = Faraday's constant

η = overpotential (volts)

R = ideal gas constant

T = temperature

Puippe also assumes that there is no concentration gradient of species from the electrode (i.e., no concentration potential), and substantiates the assumptions from other works[6,7] which are referenced as footnotes but were not read by Olsen.

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[6] J. Cl. Puippe and N. Ibl; J. of Applied Electrochemistry, **10**:775-784 (1980).

[7] N. Ibl; Surface Technology, **10**:81 (1980).

Puippe notes that the system resistance (R_T) is a function of j_F (as $d\eta_a/dj_F$). Then he defines the capacitive current:

$$j_C = \frac{dQ}{dt} = C\frac{d\eta_a}{dt} \tag{3-28}$$

and notes that

$$dj_t = 0, \text{ and } dj_F = -d_C \tag{3-29}$$

And with small enough changes in potential, $dj_F/d\eta_a$ is linear:

$$j_F = \frac{1}{A_n}\eta_a + B \tag{3-30}$$

Puippe defines A_n below, while B is a constant.

$$A_n = \frac{\eta_{an} - \eta_{a(n-1)}}{j_{Fn} - j_{F(n-1)}} \tag{3-31}$$

and

$$d\eta_a = A_n\, dj_F \tag{3-32}$$

From (3-29), (3-29) and (3-32)

$$j_C = -CA_n(dj_C/dt) \tag{3-33}$$

$$t_n = C\frac{\eta_{an} - \eta_{a(n-1)}}{j_{Fn} - j_{F(n-1)}}\ln\frac{j_{C(n-1)}}{j_{Cn}} \tag{3-34}$$

Puippe states that t_n (equation (3-34)) equals the time to change the potential over the nth interval.

From the above derivation, it is possible to quantify the time required to charge the double layer. Puippe starts with

$$j_t = j_P \tag{3-35}$$

and

$$j_F = j_P - j_C \tag{3-36}$$

Charging time (t_C) is the time for $j_F = 0.99\ j_P$. A value for t_C is calculated by summing t_n for all intervals of n until j_F equals a preset value.

In addition, Puippe gives two other ways to calculate t_c, which are not discussed here.

Finally, the double layer is expected to discharge during t_{off}, and the calculation is similar to that for charging. Puippe plots t_C vs. j_P for a $CuSO_4$ solution in H_2SO_4. He states that parameters typical for this system are α=0.5, n=2, C=50μF/cm^2 and exchange current density j_0=0.5A/dm^2. The t_C values decrease as j_P increases (log-log plot). A second plot was $\ln(aj_0t_C/C)$ vs. $\ln(aj_0t_d/C)$. When j_P/j_0 >100, the slope is -1. Puippe says this means that t_C for charging and discharging is independent of j_0. A wide range of j_0 values is possible for metal plating systems, and $Cu/CuSO_4/H_2SO_4$ can be in the A/cm^2 range if additives are used. With PC plating, high j values are experienced which means that j_P/j_0 is in the 100+ range. Often j_0 is not known, so it is good to be able to operate in the 100+ (i.e., j_0 independent) range. Puippe also states that when $j_P \rightarrow j_0$, t_c and t_d reach a constant. At $j_P/j_0 > 100$, discharging time = 7*charging time for the double layer.

If nothing is known about the system, Puippe recommends some good relations to follow:

$$t_C = 17/j_P \tag{3-37}$$

$$t_d = 120/j_P \qquad (3\text{-}38)$$

This allows for one to quickly determine optimal values for t_{on} and t_{off}.

A reality of the capacitance effect is flattening of j_F. Puippe defines this value as Δ, where:

$$\Delta = \frac{\int_{on}^{off} j_F dt}{j_m t_{off}} = \frac{j_P t_{on} - \int_{0}^{on} j_F dt}{j_m t_{off}} \qquad (3\text{-}39)$$

If there is no flattening, Δ=0. If there is complete flattening, Δ=1.

Finally, j_F can also be dampened. In this case, current efficiency is not affected, but nucleation is, because the magnitude of overpotential is changed. Puippe talks about the "magnitude of two simultaneous reactions," but does not say what they are. Increased dampening levels means that a PC waveform affects the system more like is was DC plating.

In a rough sense, Puippe considers that damping will also affect current distribution on the peaks and valleys of a rough surface. In DC plating or for a highly damped PC plating situation, the double layer will charge and the remaining current will be completely Faradaic. This current will be higher at the peaks because voltage drops with distance in a resistive electrolyte. Peaks will therefore grow more quickly than the valleys. In a system with low levels of damping, the double layer will charge and discharge more fully. Upon discharging, the energy is released as Faradaic current. Since the double layer is more uniform along the rough surface, the released Faradaic current will result in more uniform plating.

Current Distribution over the Cathode

The following is a summary from [Dossenbach 1986], beginning with a discussion on the distribution of current during DC plating. Afterwards, the effects of PC plating will be discussed.

Under the influence of a potential field between the anode and cathode, current in an electrolytic cell can be made to flow across the electrolyte. This occurs as an electron-producing oxidation at the anode and an electron-consuming reaction at the cathode. Each reaction is supported by the transport of reactive species to and/or from each electrode. In general, the field lines between electrodes are not perfectly regular. In addition, the electrode surfaces are not perfectly flat. As a result, the rate of charge transfer (or current) supported by the redox reactions can be expected to vary at different locations on the electrode.

This variation in current density is known as current distribution, and the resulting pulse-plated structures can be different from those obtained with DC plating. Dossenbach describes these differences in a qualitative manner, stating that theoretical models are very complex. The author further restricts the discussion to highly conductive electrodes, where internal variations in potential are negligible.

Three types of current distribution can be modeled, depending on the dominant mechanisms that support the electrochemical reactions. Primary current distribution completely neglects overpotential effects, and therefore only geometry may be considered. Secondary current distribution considers overpotential effects that arise from activation overpotential. Finally, tertiary current distribution considers both activation and concentration overpotential. From [Bard & Faulkner 2001], activation overpotential (η_a) arises from slow charge-transfer reactions. This tends to dominate at lower current densities. Concentration overpotential (η_c) arises from formation of a depletion zone, which must be crossed by ions traveling at a set diffusion rate.

An important characteristic of an electrochemical system is the solution resistance (R_s), especially in aqueous systems where R_s is typically larger than the internal resistance of the electrodes. Equally important is the polarization resistance at the cathode (R_p) and anode ($R_{p'}$). Dossenbach defines either as follows:

$$R_p = \frac{d\eta}{dj} \tag{3-40}$$

In addition, the overall resistance (R_t) from anode to cathode is as follows:

$$R_t = R_p + R_e + R_{p'} \tag{3-41}$$

For primary current, $R_p = R_{p'} \approx 0$ (or R_p, $R_{p'} << R_e$). Because resistance throughout the solution dominates, $R_t \approx R_s$. From the V = I * R relation, a rough cathode surface will see higher current flow through the peaks (which are closer to the anode) and lower current flow through the valleys (which are farther from the anode). While not stated by Dossenbach, one would expect that electrochemical systems with high exchange currents (i_0, due to facile kinetics) would be well-modeled by primary current. Note that a separate geometric feature can be responsible for higher local current density. It is called the peak effect, where high points are sharp enough to concentrate a large surface area for charge collection. In either case, one may expect faster deposition on the peaks and slower deposition on the valleys.

With secondary current, the redox kinetics become important. Therefore, R_p (and $R_{p'}$) cannot be ignored. With primary current, the anode-to-valley resistance (R_0) is larger than the anode-to-peak resistance (R_1). Therefore, the ratio $R_0 / R_1 > 1$. For secondary current distribution, Dossenbach adds an aggregate polarization resistance term (R) to represent the contributions of R_p and $R_{p'}$, giving $R_0 + R$ and $R_1 + R$. Since $R_0 > R$, $(R_0 + R) / (R_1 + R) < R_0/R_1$. A lower ratio of peak-to-valley resistance means a lower ratio of peak-to-valley current

density, since the two are proportional. The result is a smaller variance in deposition rate.

A common measure of the R_0 / R_1 ratio is the Wagner number (Wa):

$$Wa = \frac{R_0}{R_1} = \kappa \frac{d\eta / dj}{L} \tag{3-42}$$

where κ is the specific conductivity,

and L is the characteristic length of the system.

Dossenbach states that primary current distribution effects occur with changing Wa values. As the Wagner number increases, secondary current distribution effects become more dominant and the deposit is expected to become smoother. As mentioned, theoretical analyses are much more complex, and more than one form of Wagner number is reportedly used.

As the overpotential increases, it becomes proportional to log(j), a relation known as the Tafel equation. The rate of change of activation-controlled overpotential ($d\eta/dj$) is therefore as follows:

$$\frac{d\eta_a}{dj} \approx j^{-1} \tag{3-43}$$

This predicts lower overpotential as j increases, or less uniform deposition on the cathode. But mass-transport effects (i.e., diffusion-controlled deposition) also become more important, and Dossenbach states that this form of overpotential (η_c) is proportional to:

$$\log\left(1 - \frac{j}{j_{lim}}\right) \tag{3-44}$$

where j_{lim} is the limiting current density.

The rate of change of diffusion-controlled overpotential ($d\eta_c/dj$) is defined as follows:

$$\frac{d\eta_c}{dj} \approx \left(1 - \frac{j}{j_{lim}}\right)^{-1} \tag{3-45}$$

In this case, η_c increases with increasing j. As j increases to j_{lim}, Equation (3-42) decreases while Equation (3-43) goes to infinity. This means that $d\eta_c/dj$ will increase at high j values and the deposit should be become smoother.

As mentioned, tertiary current distribution effects include η_c as a significant contributer. From the above considerations, one would therefore expect tertiary current distribution to produce smooth deposits. However, Dossenbach states that hydrogynamic effects (as described by the diffusion layer thickness, δ) over the cathode also play a role.

In the case of tertiary current distribution, two different conditions exist. The first is described by a system whose diffusion layer thickness is greater than the height difference between surface peaks and valleys. In this case, deposition on the peaks will be faster because diffusing ions have a shorter path to travel through the diffusion layer. The second condition exists when δ is small enough to follow the surface profile of the cathode. Here the diffusion-limited transport distance is relatively constant and deposition is expected to be more uniform.

Note that the diffusion boundary layer will not be uniform for a stirred bath. This is due to the fact that the direction of electrolyte flow is constant. As such, the boundary layer (as described by fluid mechanics) will be approximately zero at the leading edge and increase to a steady-state value towards the trailing edge. Dossenbach states that j_{lim} decreases with increasing boundary layer thickness. This will therefore change the tertiary current distribtution.

The primary current distribution for DC and PC plating is the same. For secondary current distribution, Dossenbach states that the Wagner number must

be calculated using an instantaneous pulse current density. As the peak current density increases, current density uniformity is expected to suffer as predicted by Equation (3-43). Tertiary current distributions will exist if the pulse duration is long or the pulse magnitude strong enough to induce mass-transport conditions. Dosenbach relates the minimum pulse duration (τ) to the peak (or pulse) current density (j_{pk}) as follows:

$$\tau \approx j_p^{-2} \tag{3-46}$$

Finally, recall that the diffusion layer thickness (δ_p) should be as small as possible in order to allow a smooth deposit to form. Dossenbach relates δ_p to pulse duration (t) as follows:

$$\delta_p \approx t^{-0.5} \tag{3-47}$$

Chapter 4: The Sn-Cu System

Introduction

The purpose of this chapter is to introduce important aspects of the Sn-Cu binary system, and also to consider applications of pulse plating with respect to Sn and Sn-Cu. Examples are presented in order to illustrate and build upon the theory that was introduced in Chapter 3. To begin, a description of Sn-Cu metallurgy is given, with specific focus on the binary system as it relates to electronic products. Next is a review of alternate Sn-Cu materials for applications such as battery electrodes or IC circuitry. Finally, examples from the literature on Sn-Cu electrodeposition work are discussed.

Sn and Eutectic Sn-Cu

Overview

Alloys of Sn and Sn-Cu are known as bronzes, although traditionally they contain mostly Cu. In the wake of the Pb-free solder movement, Sn-rich alloys have risen as the most popular alternative [Humpston & Jacobson 2004]. In Figure 4-1, the Sn-rich portion of the Sn-Cu binary has been redrawn.

An overview of pure Sn is given by [Tan 1993], and is summarized in the next few paragraphs. Two phases exist, namely α-Sn (also called white Sn) and β-Sn (or grey Sn). The most stable phase at room temperature and above is β-Sn, which exhibits a body-centered-cubic form. Below 13.2°C, α-Sn is more stable and takes on a diamond lattice structure with much lower density and the transformation causes formation of a powder-like "pest." For most operating temperatures the transformation is slow, and it can be eliminated by adding elements such as Bi, Pb or Sb.

Sn exhibits a high (0.75V) hydrogen reduction overpotential, and dissolution in acidic or basic solutions is generally slow. One exception, however, is SO_2 with H_2O. As an ion, Sn readily exists in either the Sn^{2+} or Sn^{4+} state. In acid

solutions, either state is stable. In basic solutions, Sn^{4+} is most stable. Tan states that clear Sn^{2+} acid plating solutions exposed to air will readily oxidize to Sn^{4+} and become turbid. Sn chloride, sulphate and fluoborate salts are commonly used for plating, but the Sn ions become hydrolyzed in aqueous solutions. The hydrolysis reaction can be suppressed by the presence of excess acid in acidic solutions or excess base in basic solutions. While the descriptions are unclear, it would seem that hydrolysis in acid solutions reduces the amount of Sn^{2+} ions that are available for reduction. In addition, excess acid seems to help production of a smooth film (known as throwing power), though too much acid will degrade film continuity (known as coverage) over the cathode.

Electroplated Sn is known to form whiskers [iNEMI 2004-2]. Whiskers are long, thin crystals that grow spontaneously from the metal surface. Tan discloses a number of contributing factors that seem to affect the whiskering phenomenon, which includes the following:

- **High internal stress.** Whisker growth seems to be a stress-relaxation mechanism. See also [Zeng & Tu 2002] and [Zhang & Abys 2000], who suggest that the compressive stresses in a 2D film cause the flow of material in the third (unconstrained) dimension.
- **Coating thickness.** Tan reports that thinner coatings (1-3μm) seem more susceptible to whisker formation than thicker coatings (>8μm).
- **Organic additives.** Certain additives reportedly accelerate whisker formation.
- **Alloying.** Certain alloying elements seem to ward off whisker formation.
- **Substrate.** Metals such as Cu will accelerate whisker growth, due to the formation of Sn-Cu intermetallics with lower density than Sn. The lower density phases induce compressive stresses.
- **Temperature.** Annealing at 125-150°C for a few hours will reportedly relieve film stress and reduce the chances of whisker formation.

- **Atmospheric conditions.** Hot, humid environments accelerate whisker growth.

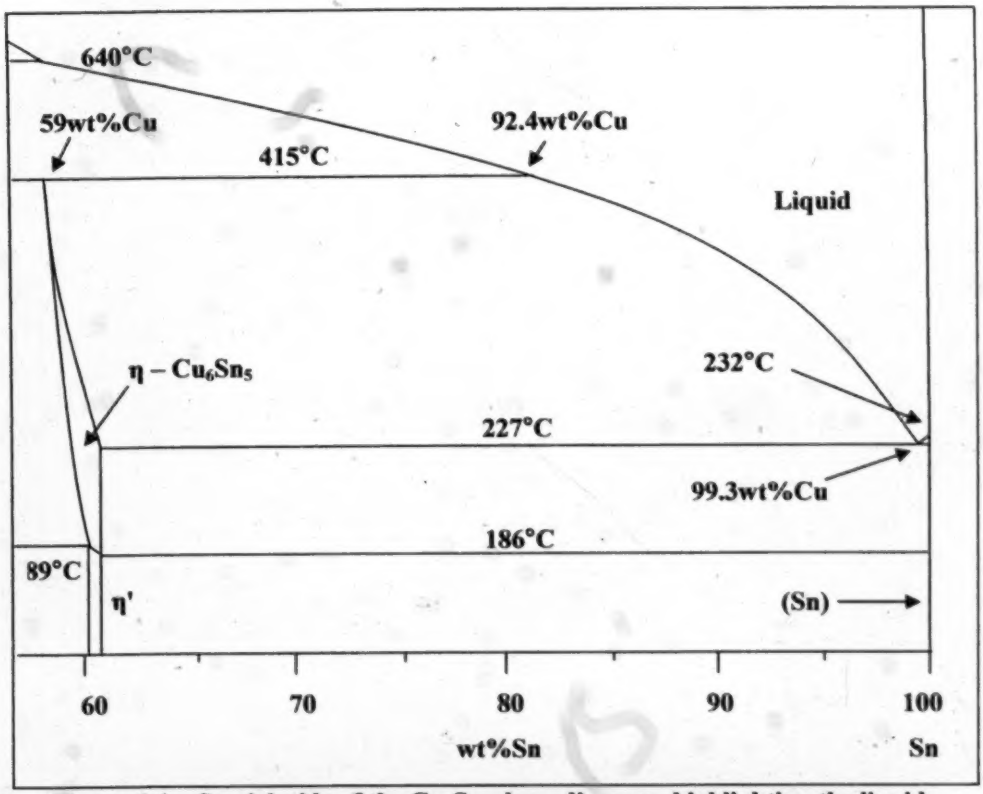

Figure 4-1 – Sn-rich side of the Cu-Sn phase diagram, highlighting the liquid, ordered and disordered Cu_6Sn_5 and pure Sn phase. Figure is redrawn from the full Sn-Cu binary after [Humpston & Jacobson 2004].

According to the work of [Saunders & Miodownik 1990] the Sn-Cu binary contains 10 separate phases, including α (0-15.8wt%Sn), β (22.0-27.0wt%Sn), γ (25.5-41.5wt%Sn), δ (32-33wt%Sn), ζ (32.2-35.2wt%Sn), ε (27.7-39.5wt%Sn), η (59.0-60.9wt%Sn), η' (44.8-60.9wt%Sn), α-Sn (pure) and β-Sn (nearly pure). For this thesis, the most important phases are η' (Cu_6Sn_5), η (Cu_6Sn_5), ε (Cu_3Sn) and β-Sn. The liquidus temperature of Sn with small additions of Cu was measured from the phase diagram, and the results are listed in Table 4-1. Note that for all cases, the equilibrium phases are expected to be pure Sn and η' (Cu_6Sn_5).

Table 4-1 – Melting point values measured from Saunders & Miodownik 1990]

Wt%Cu	T_m (°C)	Phases
0	232	Liquid + Cu_6Sn_5
1	230	
2	270	
3	310	
4	340	
5	360	
6	380	
7	405	
8	420	Liquid + Cu_3Sn

While the widespread commercial implementation of Pb-free solders is relatively new [e.g., Fukuda et al 2003-1], the formation of η' and ε intermetallic compounds (IMCs) are a well-known phenomenon. These IMCs are found when joining Cu surfaces with Sn-Pb solders, where Pb and Sn are immiscible. During soldering, liquid Sn reacts with the Cu substrate to form mainly η' [Humpston & Jacobson 2004], although the more Cu-rich ε phase can also appear at high soldering temperatures (>375°C) or in high-Pb (>75wt%) solders. According to the authors, the IMC's normally measure between 5 and 20nm, and proper imaging is therefore only possible with high-resolution microscopy. As one might expect, the location of Cu_3Sn is generally next to the Cu substrate while the Cu_6Sn_5 is found between Cu_3Sn and the Sn-rich solder.

Unfortunately, Sn-Cu IMC's are not known for high mechanical strength Humpston & Jacobson 2004] and negatively impact fatigue resistance [Harper 2005] of the alloy. As a result, it would seem that their presence should be minimized for most applications, though the authors warn that there is little evidence to conclusively tie the presence of Sn-Cu IMC's with soldered joint failure. In addition, the authors state that IMC formation is required in order to form a soldered bond. The IMC growth rate is highly dependent upon

temperature and slow growth can be expected during elevated temperature service of an electronic component.

In a separate work, [Lee & Duh 1999] consider the formation of Sn-Cu IMC's during the interaction of a Pb-free solder (Sn-1.2at%Cu-0.18at%Al-<0.02at%Ni) and a Cu substrate at a working temperature of 268°C (40°C superheat). Thermal aging was also conducted at 150°C for up to 600h. In the study, a combination of optical microscopy, secondary electron SEM analysis and X-ray analysis using an electron probe microanalyzer was used to confirm the presence of $Cu/Cu_3Sn/Cu_6Sn_5$/solder layers. They report work from other authors[1] who claim that changes in IMC thickness will affect both the mode and location of fractures within the joint. Another work that investigates the fracture toughness of Cu-Sn IMC's is that by [Balakrisnan et al, 2003].

In addition to the interface composition, [Lee & Duh 1999] conclude that the growth of the IMC's is diffusion-controlled. From their data, they argue that Kirkandall voids (from Sn-Cu interdiffusion) should be expected to form within the IMC layer, and these voids will further contribute to mechanical weakening as defects. After soldering, only Cu/Cu_6Sn_5/solder is observed. Upon ageing, the Cu_6Sn_5 IMC layer grows and eventually the Cu_3Sn phase appears. The authors determine that Cu_6Sn_5 is the stable IMC at lower temperatures. During ageing at 150°C, it is proposed that Sn diffuses into the Cu and reacts to form metastable Cu_3Sn that transforms into Cu_6Sn_5 along the Cu_3Sn/Cu_6Sn_5 interface. This transformation represents a diffusion flux of Cu that balances the Sn. A question therefore arises concerning the formation of Kirkandall voids within the IMCs, which require a flux imbalance in order to form.

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[1] D. Yao, J. Shang: Effects of cooling rate on interfacial fatigue-crack growth in Sn-Pb solder joints," IEEE Trans. Comp., Hybrid, Manufact. Technol. Part B, Vol.19 (1996) pp.154-165. The reference is given by [Lee & Duh 1999] and was not reviewed for this thesis work.

Level I Applications

The use of pure Sn and Sn-Cu seems to be fairly limited in Level I applications. In this case, the alloys must reliably replace Pb-Sn alloys with high Pb concentrations. High Pb is used so that after the Level I package has been soldered (reflowed), a Level II soldering step (second reflow) at lower temperature can be performed without harming the integrity of the Level I package [Gileo 2002]. Further, the mechanical strength of Sn-Cu joints is lower than Pb-Sn joints [Harper 2005].

However, [Karim & Schetty 2000] have demonstrated an electroplating procedure for IC bumps made of pure Sn, eutectic Sn-Cu, Sn-Ag, Sn-Ag-Cu and Sn-Bi alloys on metallized Si. In all cases, the electroplating bath contained methyl sulfonic acid and methyl sulfonic salts, with proprietary additives. Both DC and PC plating techniques were used, although the authors do not give any details. Finally, the bumps were then tested for shear strength. The procedure is shown in Figure 4-2, below.

Karim & Schetty point out that elimination of all Pb is a requirement of the RoHS legislation in Europe. However, it was mentioned in Chapter 2 that Pb is still being allowed in Level I packaging for the time being. Currently, major companies like AMD support Pb use in Level I packaging [AMD 2005]. According to AMD, this has to do with performance and reliability issues of the current material substitutes.

The features in Figure 4-2 are not drawn to scale, but note that only about 5μm thick solder layers are plated within holes of an 80 to 100μm thick photoresist. As such, one can expect that the photoresist walls may influence the mobility of electrolyte ions during electrodeposition. An extreme case is presented by [West et al 1989], who developed a one-dimensional model for pulse-reverse (PR) deposition of copper in an additive-free acid electrolyte. The authors presented the PR method as a means of achieving high aspect ratio void fill of Cu in Si IC wafers without the need of a leveling additive. They mentioned that additives are

not desirable because they are incorporated in the deposit as impurities, and also because they make the plating baths more difficult to monitor and control.

Another work of interest is [Kim & Ritzdorf 2004]. Their paper discusses the challenges of electroplating solderable bumps for interconnects on whole, 200mm diameters Si wafers. The bumps are made up of Pb-Sn (60wt%Sn-40wt%Pb and Sn-95+wt%Pb), Sn-3.5wt%Ag, 95.5wt%Sn-3.9wt%Ag-0.6wt%Cu and pure Cu, and represent a technology for wafer-level packaging (discussed in Chapter 1). While the Sn-Cu binary itself is not plated, the work is still considered to be relevant for Sn-Cu applications.

The authors discuss a competing technology that was not discussed in Chapter 3. Known as screen-printing, it is a method by which solder-containing paste is transferred through a screen or stencil by applying pressure from a squeegee. Screen printing is more of a thick film technology as opposed to thin film, and a typical stencil thickness is about 150μm. Given the ever-decreasing size requirements of a Level I package (also known as "Die-Attach"), Kim & Ritzdorf see the use of electroplating through a photo resist mask as the technology of choice.

A challenge for any electroplating system is variation in field strength between the anode and cathode. In addition, it can be difficult to obtain constant electrolyte composition over the entire cathode (wafer) surface, even when forced convection methods such as fluid circulation are applied. The authors consider how PC plating handles a real system with the above-mentioned problems.

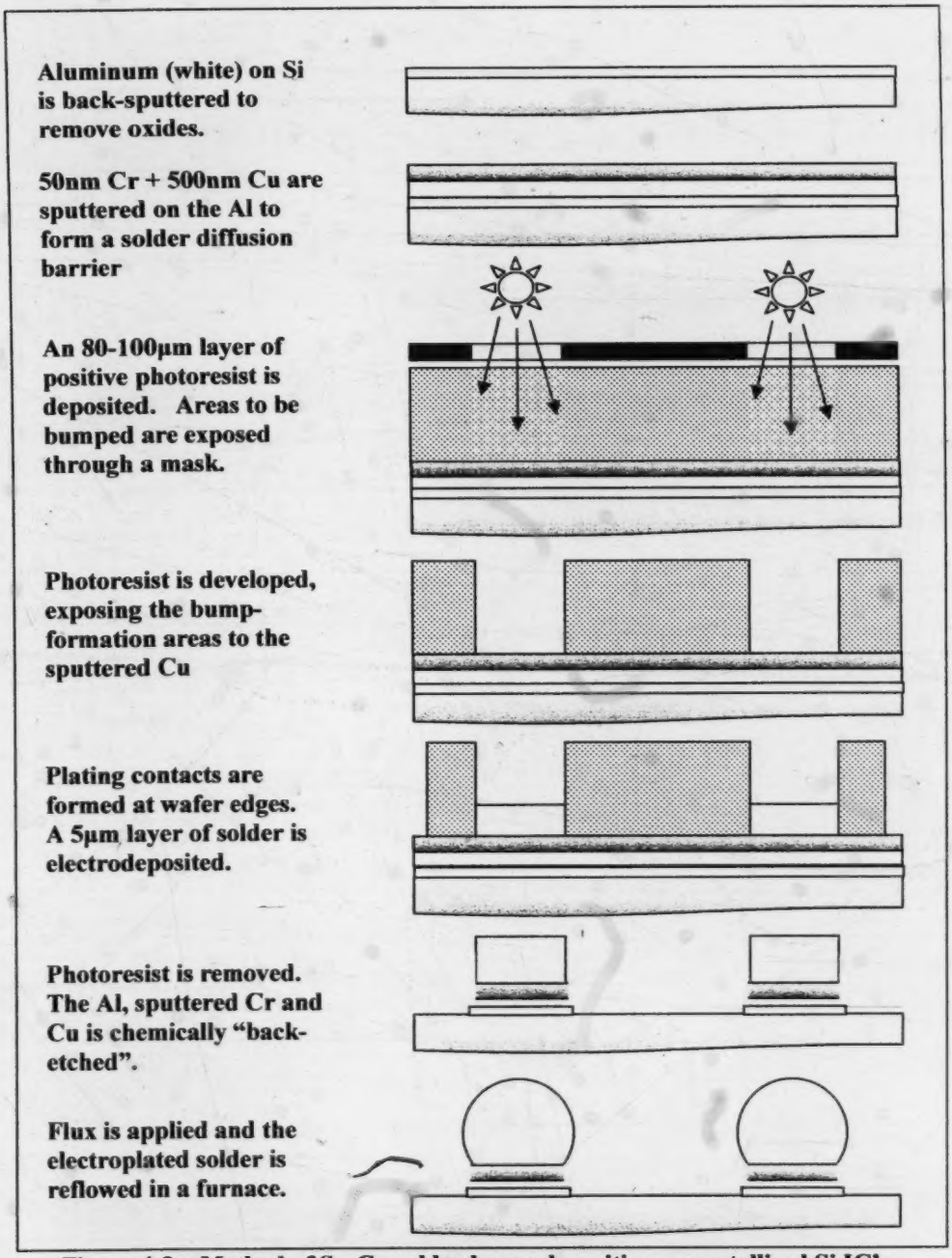
Aluminum (white) on Si is back-sputtered to remove oxides.
50nm Cr + 500nm Cu are sputtered on the Al to form a solder diffusion barrier
An 80-100µm layer of positive photoresist is deposited. Areas to be bumped are exposed through a mask.
Photoresist is developed, exposing the bump-formation areas to the sputtered Cu
Plating contacts are formed at wafer edges. A 5µm layer of solder is electrodeposited.
Photoresist is removed. The Al, sputtered Cr and Cu is chemically "back-etched".
Flux is applied and the electroplated solder is reflowed in a furnace.

Figure 4-2 – Method of Sn-Cu solder bump deposition on metallized Si IC's. Drawing is based on descriptions in [Karim & Schetty 2000].

Their experimental setup included a plating system with recirculating electrolyte at 30°C. The cathode wafer was spun like a CD at 20-60 RPM, and the spin direction was reversed every 30 seconds. In all cases a commercial (proprietary)

electroplating bath was used. A photo resist pattern was employed, as shown in Figure 4-3a, below. Further, the morphology of the as-plated bumps are shown in Figure 4-3b. Note that these bumps will be reflowed (i.e., heated above the melting point) to allow formation of spheres via surface tension effects. For PC plating, a repeating cycle of 10ms was employed.

The authors discovered that PC plating exhibited a wide range of effects on the plated bumps. In many cases features were improved, though there were instances when PC plating proved detrimental. A list is given below:

1. Shape: As shown in Figure 4-3b, the as-plated bumps took either a stud or mushroom shape, depending upon the relative thickness of the bump and the photo resist. For each shape there were three variations that are described by the shape ratio, which is the ratio of outer edge thickness to center thickness.

   For a shape ratio < 1, a dome profile is realized and the authors attribute this to the relative lack of ions near the edges during deposition. The lack of ions available for deposition may be due to blocking effects of the photo resist. In such a case, ion deposition is mass-transfer limited at the edges only, which leads to slower growth.

   For the shape ratios ≥ 1, a flat-to-rimmed profile is observed. The authors see this occurring when mass transfer effects are negligible.

   In both cases, the use of PC is expected to cause the formation of a duplex diffusion layer. The duplex layer contains a stationary layer (as seen in DC plating) and a pulsating layer between the stationary layer and the cathode. By reducing pulse duty (i.e., decreasing t_{on} versus t_{off}), the pulsating boundary layer becomes more prominent, thereby increasing the concentration gradient for the reduced species (see Chapter 3). The result is an improvement in mass transport, which allows for more uniform

deposition throughout the entire pattern.

2. Abnormal Growth: In some cases, Kim & Ritzdorf observed a third shape factor. These are called abnormal growths, and are essentially random lumps within the plated bumps. While no mechanisms for lump formation is offered, it was found that a reduction in pulse duty greatly reduced the probability of lump formation.

3. Surface Morphology: Finer grains were observed to form as the pulse duty was reduced. Note that this requires a higher peak current density in order to obtain the same average current density. Deposits with finer grains were always smoother, and this is attributed to higher adatom populations. More adatoms increase the rate of nucleation over growth, resulting in relatively finer-sized grains.

4. Film Composition: The authors consider work with Sn-3.5wt%Ag. Note that the standard reduction potential for silver is about 1 V nobler than Sn, meaning that Ag is much more likely to deposit. Smaller amounts of Ag were observed within the films with decreasing pulse duty. The effect is attributed to an increase in the partial current density of Sn, although no detailed explanation is given.

In a second study, a similar effect was observed with Pb-Sn. Note that in this case, the reduction potentials are very similar. Kim & Ritzdorf explain the effect as a change in mass transport due to strengthening of the pulsating layer (i.e., concentration gradient between the stationary layer and the cathode).

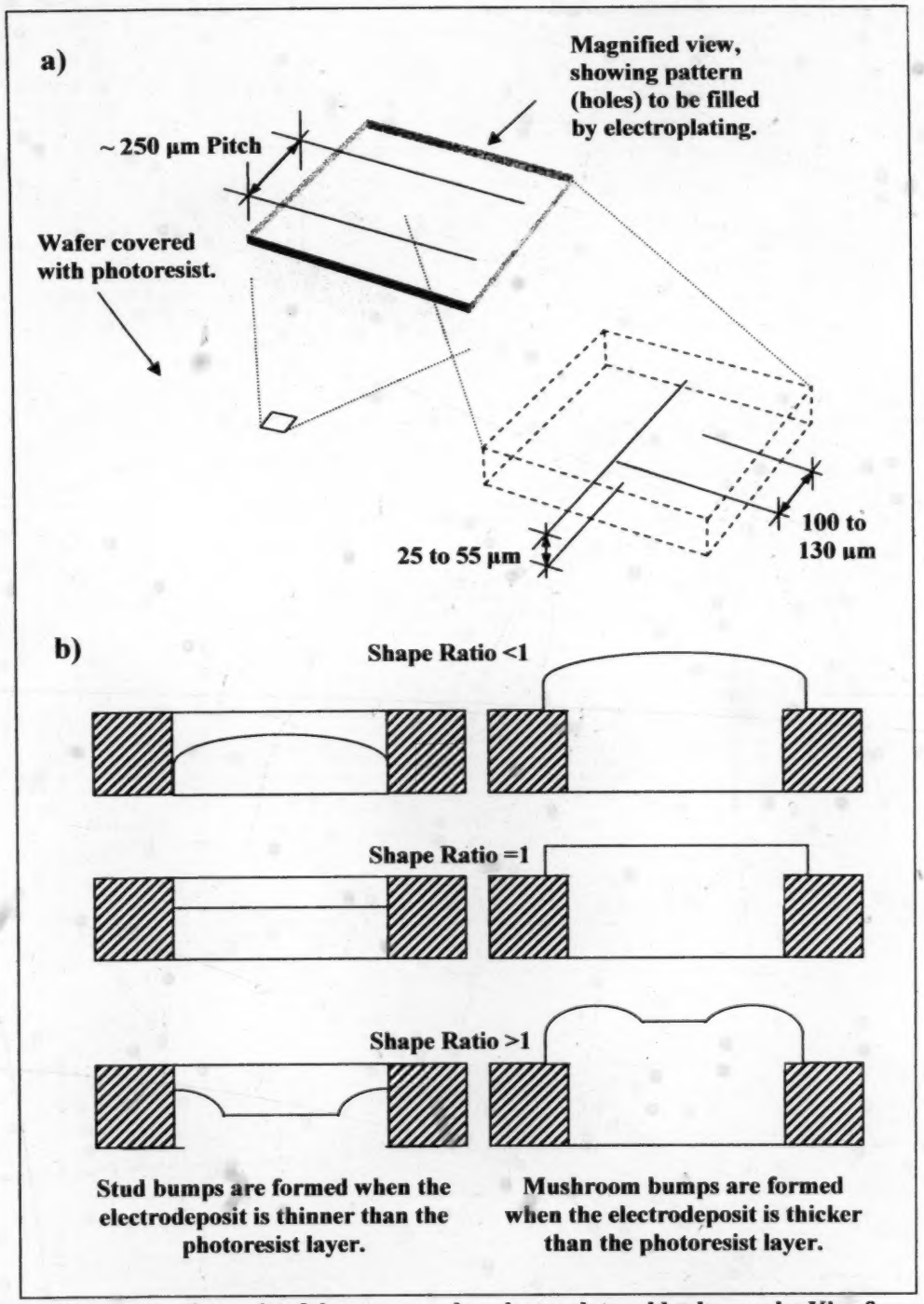
a)
Magnified view, showing pattern (holes) to be filled by electroplating.
~ 250 µm Pitch
Wafer covered with photoresist.
25 to 55 µm
100 to 130 µm
b)
Shape Ratio <1
Shape Ratio =1
Shape Ratio >1
Stud bumps are formed when the electrodeposit is thinner than the photoresist layer.
Mushroom bumps are formed when the electrodeposit is thicker than the photoresist layer.

Figure 4-3 – Example of the setup used to electroplate solder bumps by Kim & Ritzdorf. The drawings are based on figures and descriptions in the text.

5. Thickness Distribution: This effect was analyzed for variation within each bump, as well as variation among test IC's (or dies) and finally along the entire wafer radius. In all cases, the shape ratio was elevated with decreasing pulse duty. As will be seen in Chapter 5, a similar effect is observed from experiments from this thesis work.

In addition to pure Cu and Sn-rich Sn-Cu, there is interest in plating Cu-rich Sn-Cu as a replacement for pure Cu circuit traces on Si IC's. An example is the work of [Padhi et al 2003] who consider DC electrodeposited Cu-0.15wt%Sn from a sulphate bath. The Sn is added in order to reduce void formation due to electromigration and stress migration during service. As with other examples stated above, a technical challenge that had to be overcome was void-free filling of vias and trenches. An example is given of features measuring ~250 nm wide and 1000 nm deep.

Level II Applications

The following overview is based on the work of [Lal et al 2003], who investigated pure Sn and Sn-Cu as two Pb-free component finishes. The authors conducted a study of four commercial electroplating baths, two of which were designed to plate a pure Sn "matte" film and the other two as bright Sn-Cu films. In both cases, the end application was high speed strip plating of stamped phosphor bronze terminals.

A number of physical properties are of interest, because they directly impact the quality and usefulness of the deposit as a protective component coating. These are listed below, along with a brief description.

1. Thickness and Alloy Control: In this application, Lal et al plated coatings with thicknesses between 3.0 and 7.6 μm. Deposits were plated either directly over the phosphor bronze, or over a Ni intermediate layer that was

1.5 to 2.0 μm thick. The Sn-Cu films had a composition between 1.0 and 1.5% Cu[2]. No mention of acceptable thickness variation was reported.

The thickness and composition values are of particular interest for this thesis, since films with similar properties have been plated.

2. Adhesion: The authors used ASTM B571-97 for adhesion testing on as-plated samples and samples bent at 90°. All four coatings passed this round of tests.
3. Appearance and Morphology: Bright (or shiny) coatings are preferred for aesthetic reasons. These are reportedly more tarnish resistant as well. Lal et al observed the bright films to have a finer grain structure than the matte coatings. From figures provided, the pure Sn matte coatings have grain-like features measuring between ~1-8 μm. One of the coatings exhibited features that were much smaller than the other.
4. Solderability: Two types of solder were used by Lal et al were Sn matte and bright Sn-Cu coatings. These are reported to be 95.5%Sn/4%Ag/0.5%Cu and 63%Sn/37%Pb. Solder trials were conducted after plating, after 8 hours and also after 72 hours in steam. Solderability was measured using items 5 to 7, below.
5. Wetting Times: In nearly all cases, the bright Sn-Cu coatings outperformed the matte Sn coatings. Times ranged from under half a second to nearly five seconds.
6. Wetting Forces: The bright Sn-Cu coatings again did better than the matte Sn.
7. Solder Coverage: The results of these tests were more variable. One of the matte Sn and bright Sn-Cu coatings retained complete plating coverage after steaming. The other sample for each composition did not do as well.

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[2] Weight percent is assumed, but this is not specified by the authors.

For these solderability tests, Lal et al do not discuss the effects of a matte finish versus bright finish. However, they consider Cu to have a beneficial effect on oxidation resistance.

8. Susceptibility to Whisker Growth: This is probably the most interesting part of the analysis. Whiskers are spontaneous growths of Sn metal that are very thin and long. They present the danger of forming short circuits between components. Lal et al state that standardized and/or accelerated whisker growth tests do not exist, meaning that their findings may be deemed somewhat arbitrary. Nevertheless, tests were performed on samples in dry air at 55 °C, 85%RH air at 55 °C and bent samples at 85%RH air at 55 °C.

   From the tests, few trends were observed despite the fact that there was significant whisker growth. The authors were surprised to find that coatings with low carbon content and matte finish (pure Sn) were just as susceptible to whisker growth as the others.

   A common property amongst the whiskers was that they contained only Sn. Further, samples that were plated on the Ni intermediate layer exhibited fewer whiskers.

   Lal et al note that under the same tests, Sn-Pb alloys will also whisker to some extent. While no whiskers are desired, they conclude that the presence of limited whiskering over a period of six months should indicate acceptable coating performance.

9. Film Stress. This is related to whisker growth, and the absolute stresses were reported to vary with plating current density.

10. Oxidation. The oxide was reported to be SnO only, and measured from 2.5 nm in as-plated samples to 20 nm in samples that were steamed for 72 h. As mentioned, the presence of Cu was reported to enhance oxidation resistance.
11. Melting, or reflow temperature. Lal et al state that a great difficulty with many Pb-free solders is that their melting points are up to 50 °C higher than Sn-Pb eutectic. This causes problems with many of the polymer-based electronic components. A more detailed discussion is beyond the scope of this paper, and the reader is encouraged to consult the literature [e.g., Harper 2005].

While not mentioned by the authors, their data seems to suggest that the pure Sn matte coating with a finer microstructure seems to exhibit poorer solderability. However, it retains better coverage after steaming than the coating with coarser features.

An interesting article was published by [Bidin et al 2001], where matte Sn and matte Sn-Cu finishes are compared. Here, the pure Sn coating seems to perform better. They report the use of a newly-developed Sn electroplate that incorporates larger grains and a "pyramidal/polygonal structure" that is more resistant to whisker growth. This claim may be unfounded, however. In a report by [iNEMI 2004][3], no whisker-free electrodeposited Sn coatings have yet been recognized.

A number of other component (or lead frame) finishes are reported in use by Japanese industry [Fukuda et al 2003]. These include Sn-Bi, Sn-Cu, Sn-Ag, Sn-Zn, Ni/Pd/Au, Ni/Au and of course Sn-Pb.

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[3] iNEMI (or International Electronics Manufacturing Initiative) is a consortium whose mandate is involved with electronics supply chains around the World. This consortium is reportedly working on an accelerated whisker test. See http://www.inemi.org for more details.

Other Electronic Applications of Sn and Sn-Cu

Battery Electrodes

[Beattie & Dahn 2003] considered the use of PC deposited Sn-Cu films as negative Li-ion battery electrodes. The films were between 3 and 6 μm in thickness and exhibited a range of properties that depend upon the film composition. This investigation has many similarities to the work presented in this thesis. For example, a large Sn:Cu ratio is used in order to codeposit both metals. The large ratio is a result of the low Cu concentration which happens to be 0.016 M $CuSO_4 \cdot 5H_2O$, or the same level as used in this thesis. Note that the 0.016 M value happens to be 0.10 g of $CuSO_4 \cdot 5H_2O$ in 250 m*l* of solution, and is therefore a round number. Unlike the work of this thesis, Beattie and Dahn used a commercial "SnTech" solution with undisclosed composition at a concentration of 0.168 M (vs. 0.2 M $SnSO_4$ + 0.3M H_2SO_4 + no additives). In addition an extremely long, 100 s pulse cycle is employed. Nearly pure Sn is deposited at ~4 mA/cm^2 for 10 s, then nearly pure Cu is deposited at ~0.1 mA/cm^2 for 90 s and then the cycle is repeated. Within this work is a well-illustrated example of the effect of immersion plating. A Sn-plated sample was dipped halfway into the electroplating solution overnight without applied current. By the next day, the region of the sample above the plating solution was still pure Sn. The region of the sample below the plating solution had been converted into Cu_6Sn_5, as measured by XRD analysis.

Another approach to electroplating Sn-Cu electrodes for Li-ion batteries is under development at [Georgia Tech 2004][4]. In this case, both metal ions and protons are co-deposited to produce a porous dendritic film structure that is shaped by expanding hydrogen bubbles. The researchers have tailored the rates of codeposition to allow the formation of self-supporting 3D nanostructures

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[4] Meilin Liu. School of Materials Science & Engineering at Georgia Tech. The reference is given by [Georgia Tech 2004] and was not reviewed for this thesis work.

designed to maximize fluid transport and surface area. Note that it is possible to produce similar structures with the electrodeposition techniques presented in this thesis, as discussed in Chapters 5 and 6.

Traditional Plating Methods

Overview

The following section is based on the work of [Price 1983]. In general, Cu-rich alloys (or bronzes) were recognized for their commercial value. As such, most bath chemistries seem to have been optimized for alloys with only 20% Sn or less. Nevertheless, Price discusses reported applications with up to 98% Sn, so it is assumed that the traditional plating baths described below hold the potential for plated Sn-0.5%Cu films.

Cyanide (CN^-)

Historically, cyanide-based bath chemistries have been favoured for deposition of Cu-Sn. Price mentions that their development displaced commercialization efforts using an acid oxalate bath (ca. 1906) because the oxalates were sensitive to oxygen. Early cyanide baths could deposit alloys containing up to 40%Sn, although the high Sn content presented processing challenges.

Cyanide Cu-Sn baths reportedly behave much like the sulfate-Sn system, and use similar processing techniques. Temperatures are higher, though, at 60-70°C. Common ingredients include sodium or potassium stannate (i.e., Sn^{2+}), excess (or "free") alkali and excess cyanide. The excess alkali level causes a reduction in the amount of deposited Sn, while the excess cyanide increases the Sn content. Typically, Sn-Cu anodes are used, and a chemical called Rochelle salt is added to enhance the appearance and deposition efficiency of the plated layer. Other additives include organic brighteners and wetting agents. While many are proprietary, they include diethylene triamine, and glycerin. Matte deposits have been used for applications where maximum ductility is required. In such cases, Price reports the use of potassium cyanide baths without additives.

In the 1950's, the cyanide bath was augmented with stannous (Sn^{4+}) tin pyrophosphate replacing the stannate (Sn^{2+}) cyanide compounds. No mention is given as to why this bath might be considered superior, however. In addition, it is noted that the pyrophosphate bath suffered from stability problems that had to be overcome with additives.

Non-cyanide

Sulphate

Sulphate chemistry is mentioned by Price, though the author states that before the time of publication (ca. 1983) very little research was done. A number of works have been found in the literature dealing with Sn and Sn-Cu [Fukuda et al 2003-2], [Survila et al 1998], [Tzeng et al 1996], [Galdikiené & Mockus 1994], [Carlos et al, 2000], [Nakamura et al 1994-1], [Nakamura et al 1994-2], [Padhi et al 2002].

Fluoroborate

According to Price, at some time the research community determined that the best alternative to cyanide for Cu-Sn alloy plating was the fluoroborate bath. It reportedly behaves much like the pure Sn fluoroborate bath and uses similar additives. The process is also described by Price and summarized in this section.

The stannous (Sn^{2+}) fluoroborate bath is considered an improvement over stannous sulphate chemistry due to much faster plating rates. This is because the solubility limit of the Sn^{2+} compound is higher. Another major advantage is bath stability, which can be obtained without the use of additives. The bath is operated at room temperature, and additives used to control morphology are the same as for traditional sulphate chemistry: gelatin and β-napthol.

While limited information was used the [EPA DfE] (Environmental Protection Agency – Design for Environment program) attributes the presence of fluorine as cause for some environmental concern. On the very last page of [Price 1983]

there is an advertisement for a fluoborate-free[5] Pb-Sn plating bath. They simply state that fluoborates cause waste treatment and disposal problems.

Methanesulfonic Acid (CH_4O_3S)

A newer electroplating bath chemistry is based on methanesulfonic acid (MSA), and there is evidence to suggest it is an environmentally-friendly choice. According to the [EPA DfE], the chemical is biodegradable and stannous (Sn^{2+}) MSA ($C_2H_8O_6S_2Sn$) is expected to readily dissociate into the stannous ions and acid (CH_4O_3S).

BASF Corporation[6] manufactures and sells the acid, and claims that it is highly biodegradable and nontoxic. Further, MSA is reportedly less prone to oxidation than sulphuric acid. The relative difference in cost is unknown, however.

A review of DC-plated Sn-Cu and Sn-Bi films using MSA is given by [Khaselev et al 2002]. The authors comment on the traditional use of complexing agents as a way to shift the potentials of Cu (and Bi) towards Sn. This is done in order to obtain more uniform deposit composition during plating, since local current densities over a cathode can vary. Interestingly, they state that most complexing agents are being banned due to environmental concerns. Some of their early work involved sulphate chemistry, but up to five organic additives were required to stabilize the bath and produce smooth films. As a result, an MSA system was employed using additives whose activity is specific to a single ion and do not form a complex. The authors claim that the additives are environmentally friendly, allow for reliable composition control and reduce the immersion deposition reaction described earlier by [Beattie & Dahn 2003].

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[5] In this work, Fluoroborate and Fluoborate are the same chemical: BF_4^-.

[6] http://www.basf.de/basf/img/produkte/gebiete/detergents/Lutropur_MSA_engl_brochure.pdf

Khaselev et al give a partial disclosure of their Sn-Cu plating bath and operating conditions. They report the use of Sn MSA, free MSA, a wetting agent, a grain refiner and an antioxidant. Elsewhere they mention using copolymers of polyethylene glycol to deposit smooth films and derivatives of aniline to control film composition. Current densities range from 5 to 200 mA/cm^2 at operating temperatures between 20 and 35 °C. Deposited films contained 0.5 to 1.0wt%Cu.

In addition to immersion plating, a specific challenge presented by the Sn-Cu system was oxidation of Sn^{2+} to Sn^{4+}. The authors state that this oxidation reaction is a concern for all [acid] Sn systems, although the presence of Cu ions accelerates oxidation according to the following reaction:

$$Sn^{2+} + 2Cu^{2+} \rightarrow Sn^{4+} + 2Cu^{+} \qquad (4\text{-}1)$$

The reduced Cu^{+} is easily reoxidized, especially in the presence of oxygen, so that a continual supply of Cu^{2+} is available to support Sn^{2+} oxidation. The problem was overcome with undisclosed additives.

Chapter 5: Sn and Sn-Cu Plating Experiments on Au-Coated Si

A version of this chapter has been accepted for publication. K. Olsen & D. Ivey, "Pulsed Electrodeposited Sn-Cu Alloys for Use as Pb-Free Component Finishes," Sur/Fin 2005 Proceedings, June 13-16, St. Louis.

Introduction

As mentioned in previous chapters, the main purpose for the Sn and Sn-Cu film deposition work presented in this thesis is to investigate alternatives to Sn-Pb solderable finishes. The move to Pb-free presents difficulties from a plating perspective. Pb and Sn have similar reduction potentials, making electrolytic codeposition relatively easy [Zhang & Abys 2000], [Khaselev et al 2002]. A more difficult replacement is Cu, whose standard reduction potential is 0.47 V nobler than Sn.

Recall that a number of Pb-free solder alternatives exist, and that most are Sn-rich with additions of elements such as Ag, Cu, In and Bi. [Bidin et al 2001] While some properties of the Pb-free alternatives are superior, there are notable tradeoffs that prohibit the exclusive use of a single "drop-in" replacement [Suganuma 2001]. However, according to [iNEMI, 2004-2] there are two favoured Pb-free solutions exist for soldering. These are eutectic Sn-Cu for wave soldering and Sn-3.9wt%Ag-0.6wt%Cu ±0.2% for surface mounting. Sn-Cu itself is known to be a solderable alloy with good resistance to tarnish [Bidin et al 2001], [Khasev et al 2002] although there is a great deal of concern with the alloy's resistance to whisker growth [Swanson & Zhang 2002], [Tan 1993], [Lowenheim 1978].

In addition to solders, solderable surfaces should also be Pb-free. This chapter considers the development of a pulse-plating bath and process for depositing Sn-Cu films on Au-coated Si. As such, the solderable finish would have a composition that closely

matches the solder. In the next chapter, the deposition of similar films on wrought Cu and Cu-coated Si substrates will be presented.

Obviously, any finish with commercial potential will have to exhibit good resistance to whisker growth. While this may be possible through a carefully-engineered set of plating conditions [Bidin et al 2001], such an approach is beyond the scope of this thesis. Some of the more popular Pb-free finishes include Ni-Pd-Au and pure Sn over Ni on a Cu substrate, and iNEMI reports fewer tendencies for whisker growth with such material systems.

As a baseline for quality assessment, an acceptable Sn-Cu film should exhibit a number of criteria [Tan 1993], [Price 1983]. These are listed below:

1. A smooth, bright surface: This criterion is mostly cosmetic, but reflects good surface coverage and efficient use of the electroplated material.
2. Resistance to edge effects: The electric field surrounding a cathode is much higher across a sharp corner than it is over a flat surface. Plated parts with such features must not exhibit dendritic or whisker-like growth here. It is expected that a system capable of plating smooth deposits over a wide range of average current densities will exhibit good resistance to edge effects.
3. Complete, consistent surface coverage: This is required to protect the substrate from tarnish. Film coverage should also not be overly thick at the edges or too thin at its center.
4. Eutectic composition: For Sn-Cu, this occurs at 0.7% [See Figure 4-1, Chapter 4]. A eutectic film will have the lowest possible melting point, and will not exhibit separate liquidus and solidus temperatures. When these two values are different, a "mushy" temperature zone can be expected. Ideally, the composition should be constant and independent of current density.
5. Consistent composition: Small variations in the Cu content of a film can greatly increase the liquidus temperature of a Sn-Cu film. In general, consistency in

composition is desirable [Bidin et al 2001], and should give the film more predictable soldering performance in an industrial application.

6. Resistance to whisker growth: No comprehensive whiskering test exists [iNEMI 2004-2]. However, one should expect that a low degree of compressive film stress is desirable [Zeng & Tu 2002]. Further, [Zhang and Abys 2000] report that the optimal grain size for a whisker-resistant, Sn-rich film is between 1 and 8 μm. If the grain size is smaller, grains will deform to reduce the energy contained in grain boundaries. Because the 2D films are not restricted from movement above their surface, whiskers readily grow outwards.

While technology exists to produce such films, many such plating baths require the use of complexing agents that are highly toxic (such as CN^-) [Tan 1993], [Price 1983], [Lowenheim 1978] or present difficulties with waste treatment due to ion complexing [Muramatsu 2002]. The aim of this research effort was to employ a low-or-no additive plating bath with low environmental impact, and to attempt to meet as many of the above criterion as possible.

A similar grid was also plated using pure Sn. In addition, a third grid was constructed to illustrate the effects of moderate agitation. Finally, experimental work was undertaken on enhancing the shelf life of the standardized solution with citric acid.

DC and PC Deposition of Sn and Sn-Cu Films

Experimental Procedure

Overview

A sulphate-based chemistry was chosen for this work, because it met a number of criteria. To start, it has a well-established record of use with both Sn and Cu [Tan 1993], [Price 1983], [Lowenheim 1978]. Acid-based Sn-plating solutions use Sn^{2+} ions for cathodic reduction, and therefore consume less energy. By and large, a sulphate bath can

be easy to control during electrodeposition, and the chemicals are not overly hazardous. Finally, sulphuric acid and metal sulphates are readily available at low cost.

The original goal of this research was to develop an additive-free sulphate solution for use with a pulsed square waveform. Such a technology would be attractive to an industrial user, especially since traditional additives are difficult to monitor in solution and need to be replenished [Tan 1993]. The same reference also correlates the presence of additives with carbon content within the deposits, which inhibits solderability. In addition, no complexing agents were added.

In addition to this work, other research groups have developed DC plating baths whose compositions are publicly disclosed. For example, [Fukada et al 2003] use 2 M H_2SO_4, 0.2 M $SnSO_4$, 0.02 M $CuSO_4 \cdot H_2O$ and polyoxyethylene lauryl ether (POELE) as an additive. The role of the POELE is reportedly as a grain refiner, although no data is given on roughness. POELE is quite expensive - over US$100 per gram. A more complex recipe is offered by [Muramatsu et al 2002], who specify a list of acid media (including H_2SO_4), a Sn^{2+}:Cu^{2+} ratio between 10 and 100:1 and thiourea or a thiourea compound to act as a stabilizer. In neither case is a pulsed current specified.

A series of preliminary experiments were carried out and it was found that promising deposits could be obtained at low H_2SO_4 concentrations. The rationale behind low levels of acid is cost and environmental impact. Table 5-1 outlines the standard bath chemistries used for this work. The amount of charge transferred to the cathode was fixed at 30mA*min. For Grid I, an unagitated standard solution was used. For Grid II, experimental conditions were similar, except that no $CuSO_4 \cdot 5H_2O$ was added. For Grid III, the standard solution was agitated by stirring with a glass impellor at 200 RPM. All these samples were plated on Au seed layers.

Table 5-1 – Composition and conditions of electroplating baths for this work.

Grid	Component	Concentration mol /	Concentration g / (oz gal)	Agitation
I "Standard"	H_2SO_4 $SnSO_4$ $CuSO_4 \cdot 5H_2O$	0.2 0.2 0.0016	29.4 (0.81) 43.00 (1.18) 0.40 (0.011)	0 RPM
II	Same as I, but no Cu			0 RPM
III	Same as I			200 RPM

Three main experimental grids were developed. Within the grid, the pulse duty (p) and average current density (j_{avg}) were varied. Pulse duty is defined as:

$$p(\%) = \frac{t_{on}}{t_{on} + t_{off}} * 100 \qquad (5\text{-}1)$$

Here t_{on} represents the time increment during which the deposition overpotential is applied. The time increment during which no deposition occurs is t_{off}. The sum of t_{on} and t_{off} is the total cycle time. In this work, the total cycle time was fixed at 10 ms.

As the pulse duty decreases, the peak current density increases according to Equation 5-2.

$$j_{pk} = \frac{j_{avg}}{p} \qquad (5\text{-}2)$$

After electroplating, each Au-coated cathode was removed from the solution and rinsed with distilled water. It was then placed in acetone, in order to remove the plating mask.

Electroplating Bath

The following procedure describes the method used to plate and characterize the standard grid. Note that in preliminary experimental work performed by Olsen for this thesis, the minimum film composition was about 1.4% Cu, and ideally this should be 0.7%. As a result, the concentration of $CuSO_4 \cdot 5H_2O$ was reduced 20% from 0.0020 M

(0.1258 g per 250 m*l* batch) to 0.0016 M (0.1000 g per 250 m*l* batch). The components used are as follows:

1. 250 m*l* of 0.2 M H_2SO_4
2. 10.74 g of $SnSO_4$
3. 0.10 g of $CuSO_4 \cdot 5H_2O$

The 0.2M H_2SO_4 solution was prepared from 2.0M acid as follows:

1. Add 50 m*l* of 2.0M H_2SO_4 to 383 m*l* H_2O.
2. Mix well without shaking.
3. Store in a labeled 500 m*l* Nalgene® bottle.

A quantity of 2.0 M acid was stored in a second labelled 500 m*l* Nalgene® bottle, and prepared from concentrated H_2SO_4 as follows:

1. Add 56 m*l* concentrated H_2SO_4 to ~400 m*l* of H_2O in a 500 m*l* florence flask.
2. Carefully add enough H_2O to bring the level up to 500 m*l*.
3. Allow to cool to room temperature overnight before use.

These procedures were followed for every experiment, in order to maintain consistency. For example, a batch was never halved or doubled. Care was taken not to shake the solutions so that extra air would be dissolved into the water, although no steps were taken to remove dissolved air, either. All materials were weighed to at least 0.1 g accuracy, while the liquid volumes were within 0.5 m*l* accuracy per 100 m*l* of liquid volume.

Au Substrate (Cathode) Preparation

Initial work focused on the deposition of Sn-Cu alloys on Au-coated Si wafers. Au was used for initial work, because it allowed for the determination of coverage via energy dispersive X-ray (EDX) analysis. The Au layer was sputter deposited to about 250 nm thickness. Between the Au and Si was a 25 nm Ti adhesion layer. Because the Si wafers

were polished, the Au layer was mirror smooth. Each wafer was rinsed with isopropyl alcohol, and then cleaved into pieces measuring about 1 cm by about 2 cm.

Plating areas measuring 0.3 x 0.3 cm were marked on Au-coated Si wafers using a fine-tipped felt pen. They were then masked with a red stop-lacquer that has been used successfully by Ivey's group for other plating work. The accurate application of the lacquer is difficult, since the viscosity is a strong function of dissolved acetone. The acetone evaporates quickly, and must be continually replaced. The masking material was applied using a small strip of card stock measuring about 1cm wide. If the film was too thin, holes would appear after drying. The resulting variance in plating areas was most pronounced with the standardized grid (samples denoted by F1-x). As time went on, the author's skill improved and so did the variance in plating areas. As will be seen, the variance for the pure Sn grid and stirred grid is much better. The purpose of the mask was to prevent electrodeposition and current transfer outside of the plating area, or on the edges of the Au-coated Si. A photograph of typical electrodes is shown in Figure 5-1.

Figure 5-1 – Examples of a Pt-coated Si anode (above) and a Au-coated Si cathode (below).

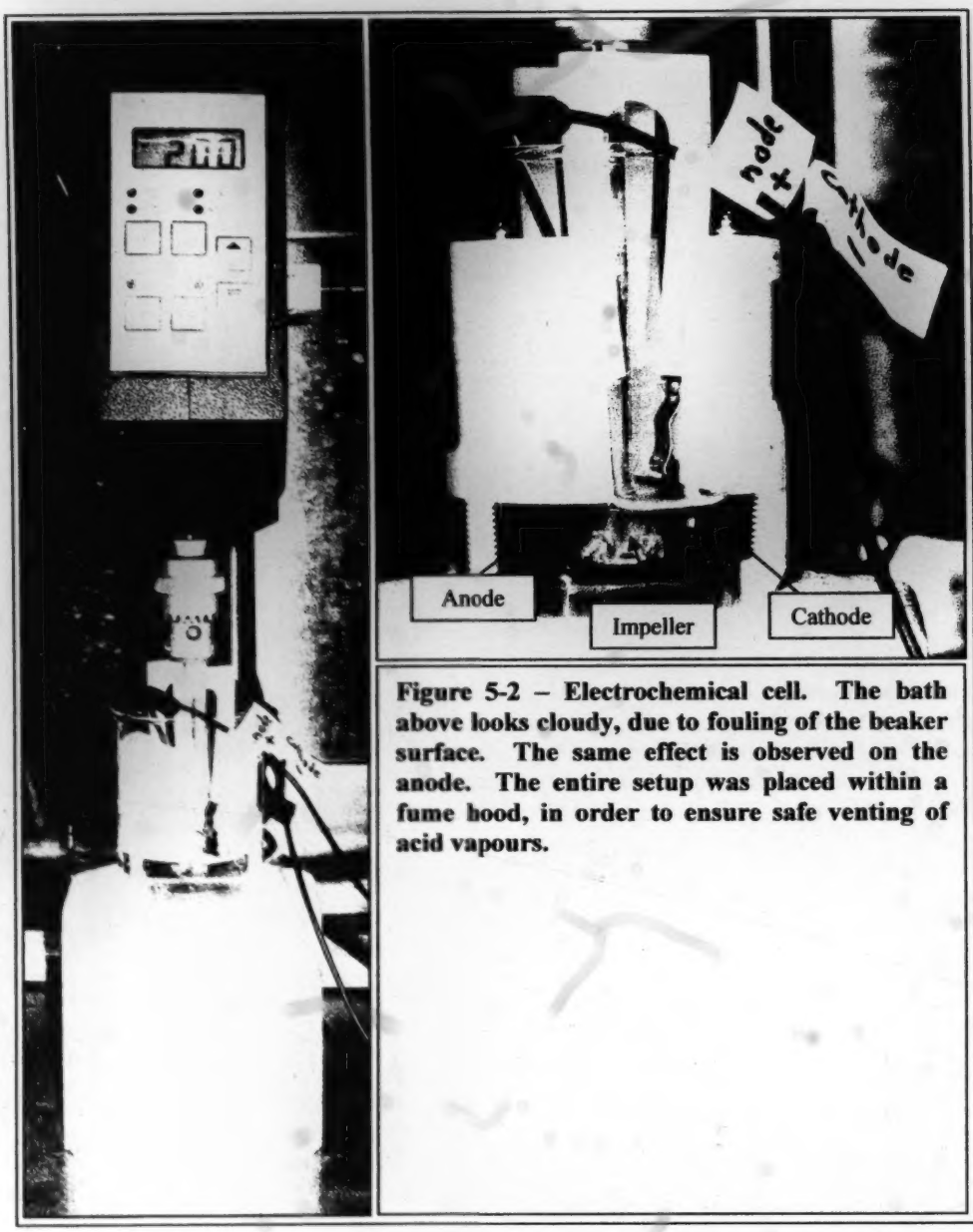

Figure 5-2 – Electrochemical cell. The bath above looks cloudy, due to fouling of the beaker surface. The same effect is observed on the anode. The entire setup was placed within a fume hood, in order to ensure safe venting of acid vapours.

Finally, all waste material was stored in a polypropylene bucket with a sealable lid. The contents were marked and disposed of according to University regulations.

Experimental Setup and Procedure

An example of the experimental setup is shown in Figure 5-2. In order to avoid confusion, the Pt-sputtered anode was always placed on the left-hand side, and the Au or Cu cathode was always placed on the right-hand side. The white plastic electrode holders are made from machined polypropylene, and are the same as those used by other researchers within Ivey's group. The standard polypropylene container was replaced with a Pyrex® beaker in order to maximize visibility of the cathode surface during electroplating. A drawback of the beaker was the fact that it contains a slight taper. This caused the bottom edges of the electrodes to be a few millimeters closer than the top edges. Because the air refresh rate of the lab was unknown, all plating experiments were carried out in a fume hood. This way sufficient ventilation of any acid vapours was assured. Use of the fume hood was also handy for dispensing chemical powders; Si wafer cleaning can produce many small Si fragments and all surface preparation operations that involved the use of solvents.

For additive-free electrolytes, all surfaces except the cathode developed a yellow film. This was difficult to clean, and required extended immersion in an ultrasonic bath. A residue-free detergent (Sparkleen®, Fisher Scientific) with warm tap water was used for cleaning the beaker, glassware and polypropylene holder. After thorough rinsing, each item was rinsed three times in distilled water. Anodes were not cleaned, and instead a new anode was used for each plating experiment. Anodes were made from cleaved Si wafers that were coated on one side with sputtered Pt on top of a Ti adhesion layer. The anode and cathode were placed in separate polypropylene holders inside a 250 ml beaker. The anode to cathode area ratio was variable, but in all cases was at least 1:1. The distance between the electrodes was 2.4 cm.

A programmable Dynatronix PDPR power supply was used for all plating experiments. The system was wired as shown in Figure 5-3, below. A capacitor was added in series in order to reduce high-frequency noise from the power supply. Even so, the signal was

very noisy, and the error measured across the oscilloscope was as much as ±50% of the setpoint value at low (~<10 mA) current output. For most plating conditions, however, the error was within 10%.

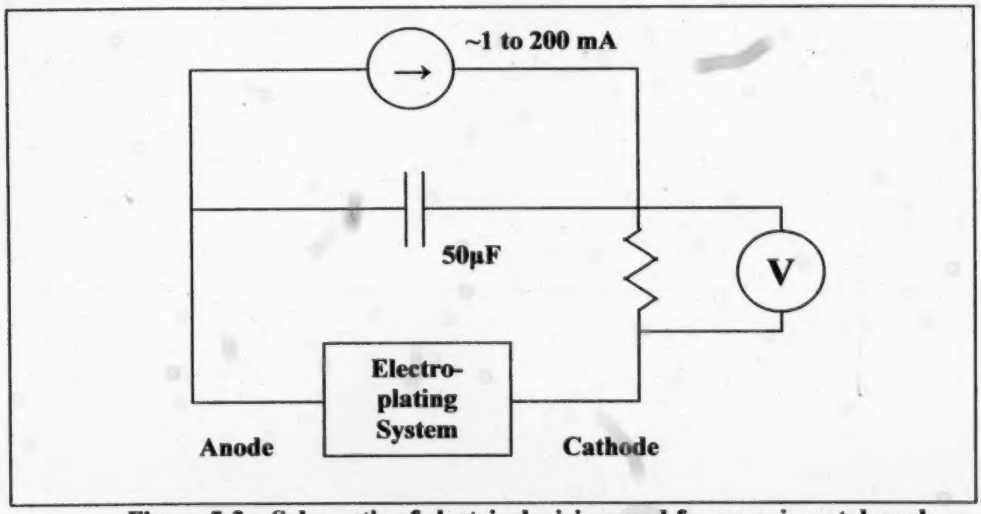

Figure 5-3 – Schematic of electrical wiring used for experimental work.

Before running the experiment, the electrical leads that would be connected to the electrodes were shorted together and the power supply activated. A circuit trace would appear on the scope, and characteristics of the square wave pattern were recorded on the data sheet. In addition, signal variance from the set point and zero values were recorded. Note that the oscilloscope displays voltage values, which can be converted to current values by using the following equation:

$$i = V / R \qquad (5\text{-}1)$$

where i is current (mA);

V is the voltage readout on the scope (mV);

R is the resistance shown in Figure 5-3 (50.0 Ω).

$$j = i / A \qquad (5\text{-}2)$$

where j = current density (mA/cm^2);

A is the measured area of the cathode (after masking, cm^2).

After testing the power output, about 60m*l* of electroplating solution was poured into the beaker (preassembled with the electrodes and holders) and the wires attached to their corresponding electrodes. If stirring was required, then the stirrer was turned on at least 5 seconds before activating the power supply.

Microstructural Analysis

All microscopic work was carried out using a Hitachi S2700 scanning electron microscope at 20kV and a working distance between 16 and 18 mm. Images of all samples were taken in plan views at 200X (200 μm bar on the images) and 50X (500 μm bar on the images). If the film was of particular interest, higher magnifications were also employed in order to document fine microstructural features. In addition, the Au-coated Si wafers were cleaved in half to reveal a cross-sectional (or edge) view of each sample. All cross-sections were recorded at 200X (200 μm bar on the images), and 1000X if the film was exceptionally smooth.

EDX Analysis of Coverage and Composition

For all samples except a few from the F1-x grid, an area measuring about 600 x 425 μm at the centre of each sample and analyzed for 100 seconds. The probe current was set to 0.59 nA, with the beam strength set at 14 (arbitrary units) and a 17 mm working distance. For a handful of samples an area approximately 4 times larger was utilized, but each spectrum was collected for the same time. Some samples were analyzed at both the small

and large areas, and the results from each analysis were within the reported precision of the EDX system. As such, no effort was made to reanalyze the large-area samples.

After an EDX spectrum was collected, quantitative analysis was carried out for relative concentrations of Sn, Cu and Au. A second quantitative analysis was run, but only for relative concentrations of Sn and Cu. The quantitative program uses calibration standards.

In an attempt to quantify film coverage plated on Au, the EDX peaks corresponding to Sn, Cu and Au were measured using EDX analysis and normalized. In a few cases S was also detected, though this was for plating trials using citric acid. Coverage data was taken as the sum of wt%Sn and wt%Cu (or 100wt% - wt%Au). Later, only the Sn and Cu peaks were used to obtain relative (wt%Cu versus wt%Sn) concentrations for deposit composition.

XRD Analysis

A few samples were analyzed using the Rigaku Rotating Anode XRD, model RU200 with a thin-film camera. These samples were plated under various conditions using a bath that contained a 10:1 ratio of Sn^{2+}:Cu^{2+}. Data was measured at $\theta = 4°$ from $2\theta = 20°$ to 90°.

Results and Discussion

PC Plated Morphology on Au-coated Substrates

In this work, samples were plated using the unagitated, standardized plating solution (Grid I). These included samples plated at j_{avg} = 5, 15, 30, 50 and 70 mA/cm^2. For each constant pulse duty, a critical average current density ($j_{avg,c}$) was observed. Above this value, the deposit was highly dendritic. At 100% and 50% pulse duty, $j_{avg,c}$ is between 30 and 50 mA/cm^2; at 20% and 5% pulse duty, $j_{avg,c}$ is between 50 and 70 mA/cm^2.

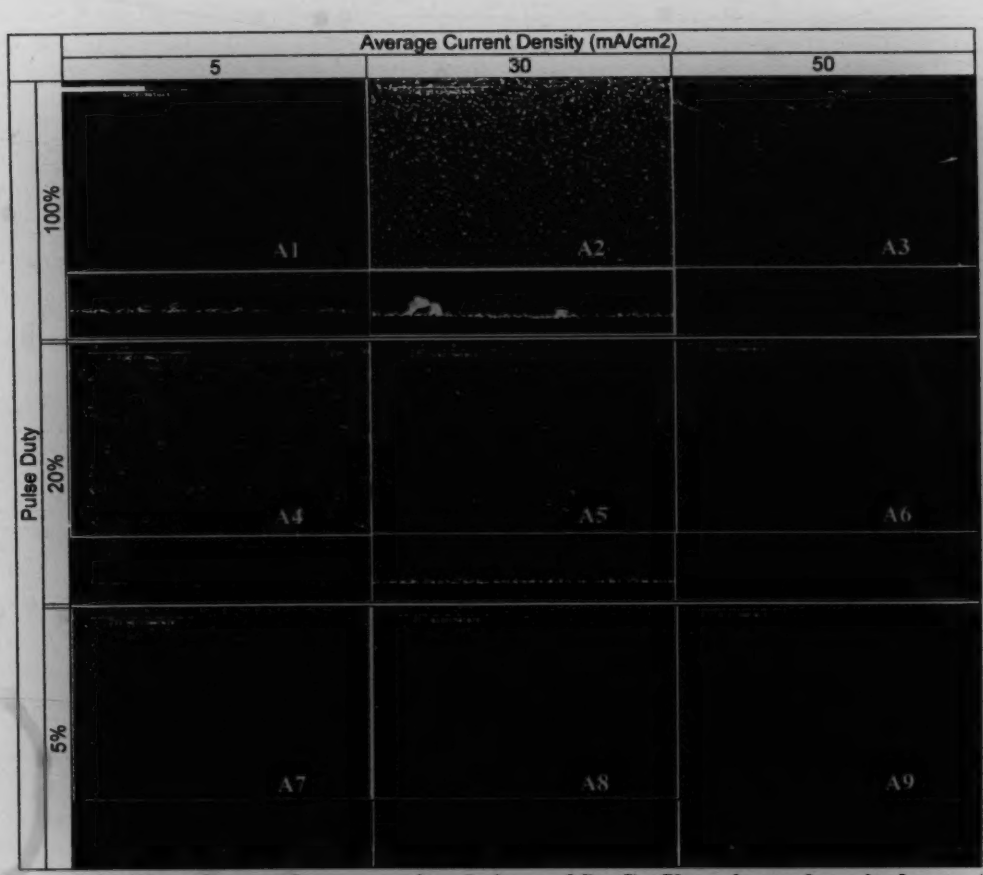

Figure 5-4 – Plan views and cross sectional views of Sn-Cu films electrodeposited onto Au-coated Si. The plating bath was not agitated. Surface coverage, feature size and film roughness are all functions of pulse duty and average current density.

Figure 5-4 is a composite photograph of nine samples. They are arranged in a grid to show the effects of average current density (left to right), and pulse duty (top to bottom). Each sample is labeled from A1 to A9, and both a plan and cross-sectional view are given. Note that a pulse duty of 100% is simply DC plating. For all samples, a fixed current of 30mA*min was deposited. Due to the manual masking procedure, the ratio of current per unit area varied. Average current density was controlled by measuring the area of each sample, and programming the power supply accordingly.

Clearly, there is a trend regarding the degree of coverage. The plan views give a good indication of how much of the Au substrate is covered, as well as the average feature size. Note that higher pulse duty and lower average current density yield films with poorer coverage and more agglomerated deposits. It is not known whether these agglomerates are composed of single Sn-Cu grains, however. From the cross-sections, it can be seen that the relief is greater for films made of larger agglomerates, such as A1.

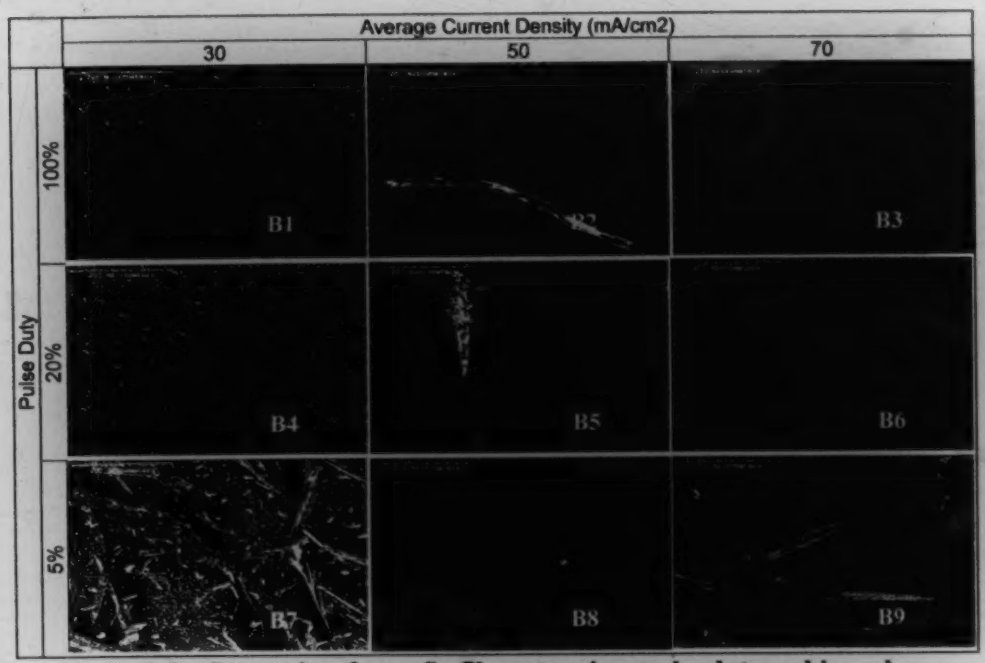

Figure 5-5 – Composite of pure Sn films at various pulse duty and j_{avg} values. The scale bars are 200 μm wide.

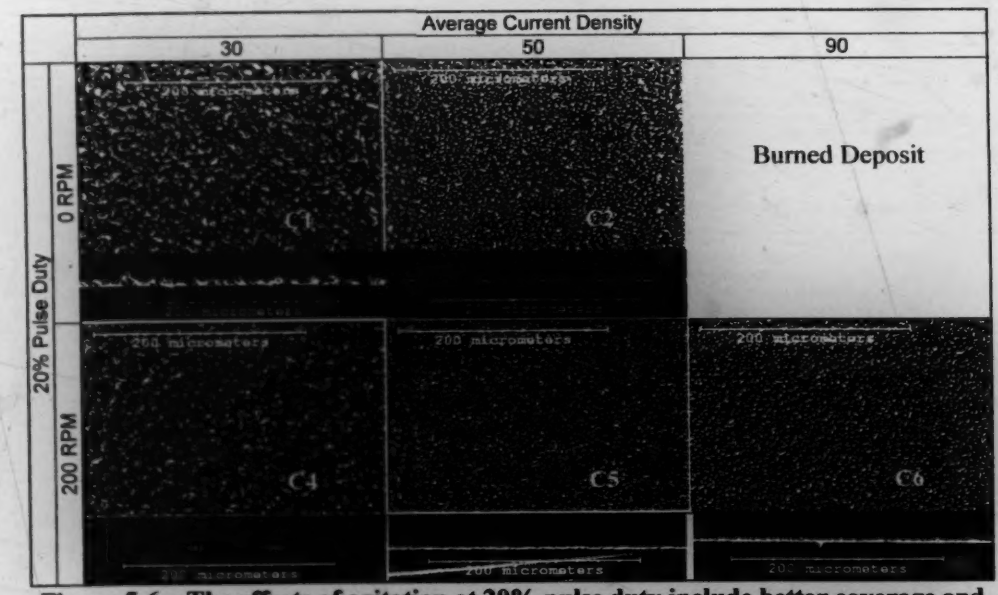

Figure 5-6 – The effects of agitation at 20% pulse duty include better coverage and flatter films. Higher critical average current density allows faster plating and lower Cu content.

Figure 5-5 is a similar composite photo showing the effects of average current density and pulse duty using pure Sn (Grid II). The best film is B6. Note that the j_{avg} values are much higher than in Figure 5-4, suggesting that Cu^{2+} limits the maximum plating current. This makes sense if one considers that the $Cu^{2+} \rightarrow Cu$ reduction is nobler than $Sn^{2+} \rightarrow Sn$ reduction. Trends similar to Figure 5-4 are observed regarding coverage, while the most noticeable difference is the existence of whisker-like dendrites. These structures have few, if any, branches and were observed in the SEM within hours of plating. They are most prevalent at low pulse duty. Some of the whisker-like dendrites were as long as 5mm.

Finally, the standard solution was stirred moderately using a small impellor rotating at 200 RPM. A comparison of agitated and non-agitated conditions is given in Figure 5-6, and shows that this level of agitation has both a refining and leveling effect. Stirring enabled smooth films to be plated at higher average current densities.

Coverage was also observed to be a function of location, as shown in Figure 5-7. At lower average current density, the coverage decreases towards the center of the film. Edge definition is poorer with increasing average current density because of dendritic growth. This suggests that the range of current densities from which a smooth, well-covered, dendrite-free film can be deposited is narrow. The edge definition observation also supports the observations of [Kim & Ritzdorf 2004] as stated in Chapter 4. To summarize, the authors found that the film roughness generally decreased with decreasing pulse duty. However, the trend was reversed near the edges of the masked plating area.

Using the EDX data, two separate plots were generated for coverage versus j_{avg} for 5% pulse duty and DC data. These plots are shown in Figures 5-8a and b. Note that the 5% pulse duty data points show high coverage for all values of j_{avg}. In contrast, the DC films seem to follow a trend of increasing coverage with increasing j_{avg}. For the 5% pulse data, the pure Sn films (hollow triangles) exhibit the highest coverage values. However, the Sn-Cu films deposited from the unstirred solution (hollow diamonds) are the most consistent. During experimental work, it was noted that at moderate current densities (i.e., around 30 mA/cm^2 for Grid I samples) increased plating times tended to improve coverage. However, at very high and very low current densities, increased plating times yielded granular or dendritic films whose features did not flatten out on the substrate. Therefore, coverage was poor to begin with and did not improve.

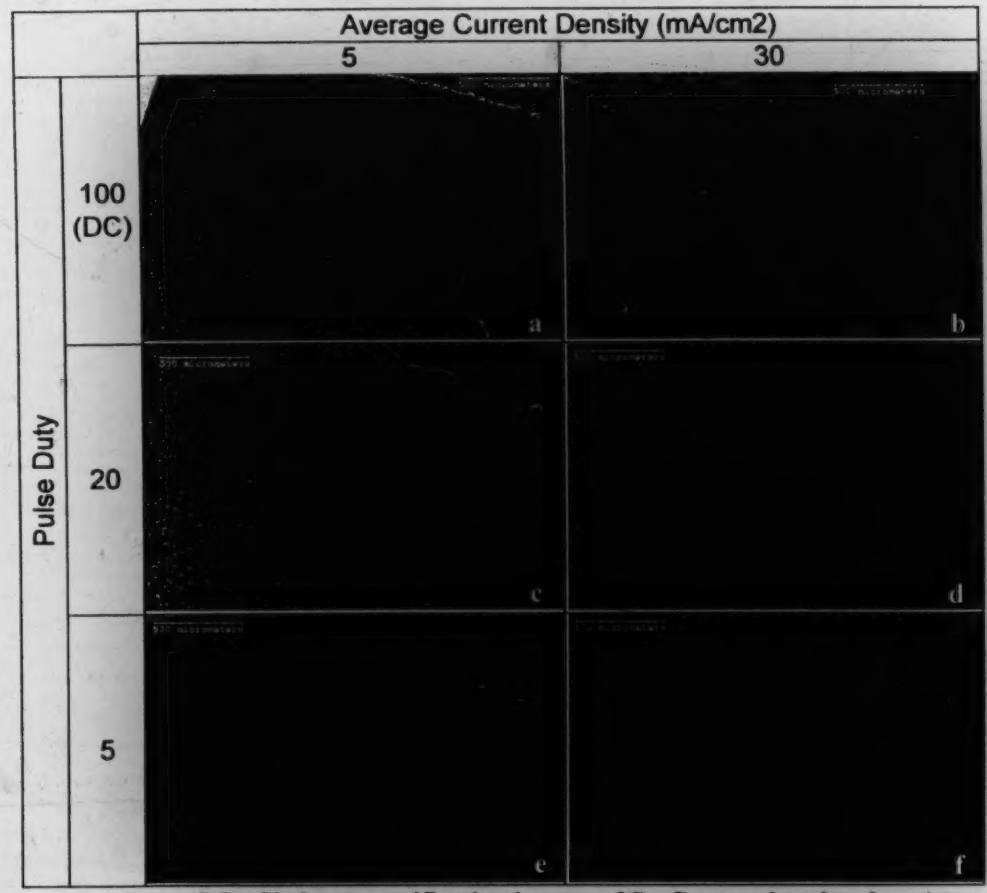

Figure 5-7 – Six low-magnification images of Sn-Cu samples plated on Au at variable pulse duty using an unagitated bath (Grid I).

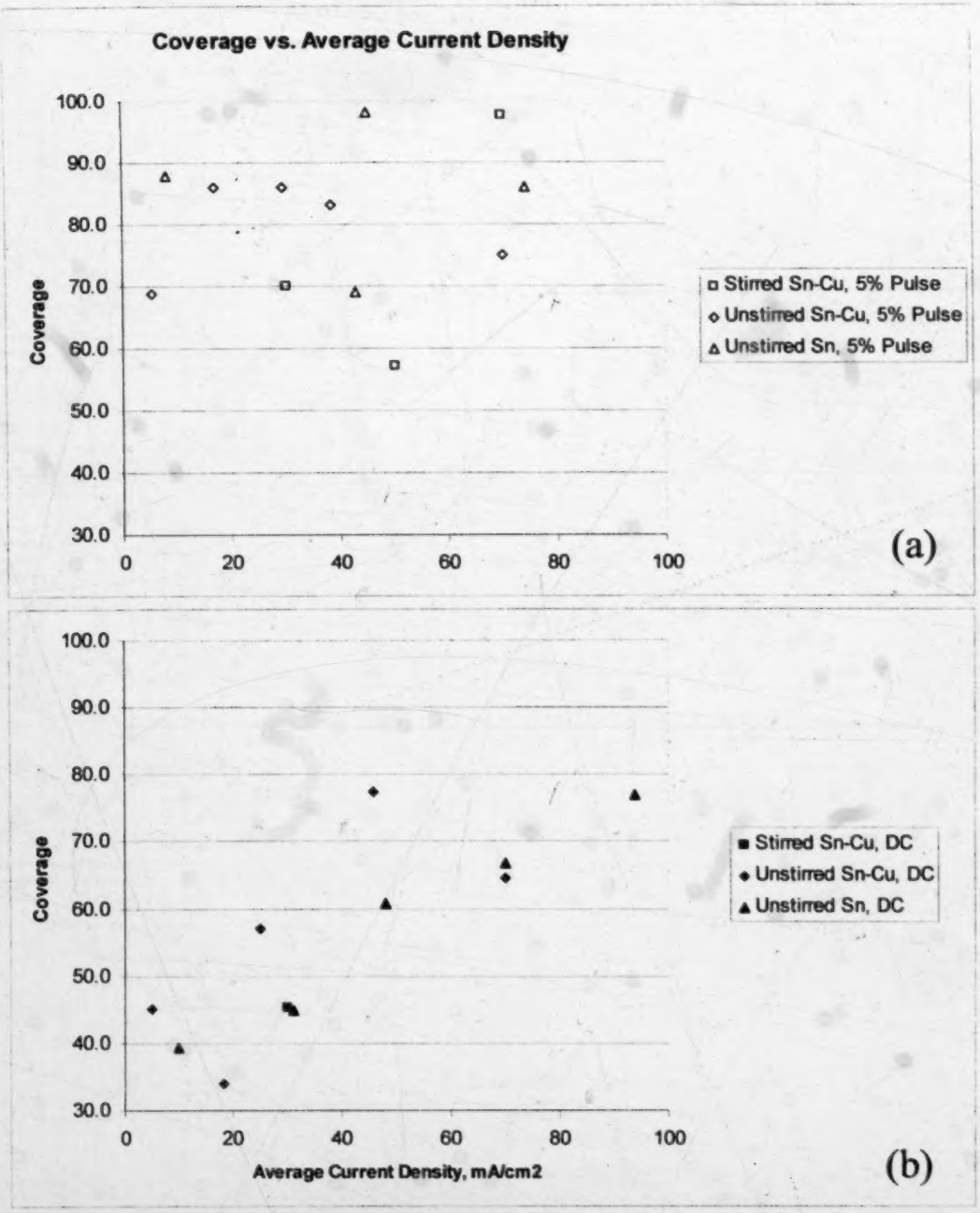

Figure 5-8 – Coverage plots, showing that 5% pulse duty films (a) tend to have better coverage than DC films (b). DC films show a linear trend for coverage vs. average current density. Measurement error limits are within the symbol size.

For the DC (100% pulse duty) plots, the Sn-Cu films deposited from unstirred solutions (solid diamonds) had the highest coverage values at moderate current densities. The most consistent trend belongs to pure Sn deposited from the unstirred solution (solid triangles).

Given the scatter, it is difficult to draw any conclusions. Therefore, one cannot say whether the presence of Cu or the use of agitation affects coverage. The clearest trend is a linear relationship between coverage and average current density for DC-plated films. Also, the 5% pulse duty films yield consistently better coverage.

Note that there was a large variance in plated areas amongst the samples. In an effort to determine whether such variance caused the large scatter, the coverage data in Figure 5-8 was normalized as follows:

$$c_{norm}(\%) = c_{raw} \frac{A_{meas}}{A_{max}} \cdot 100\% \qquad (5\text{-}3)$$

Where c_{norm} is the normalized coverage (in percent)

c_{raw} is the actual coverage value determined by EDX analysis

A_{meas} is the measured plating area

A_{max} is the largest measured plating area

Given the fact that a constant amount of charge (30 mA*min) was transferred, a constant amount of Sn and Cu is deposited. Note that the applied current densities were adjusted according to the measured surface areas. It was impossible to adjust the amount of charge in a similar fashion because the power supply only measured current transfer in 10 mA*min increments. If the plating area is relatively small, one would suspect that the resulting film would be thicker and therefore the measured coverage value would be artificially high. In the same respect, plating over a relatively large area would produce a

thinner film, which might lower the real coverage. In the future it would be best to control the current transfer by elapsed time, though this requires an adjustment for variable current density.

For pure Sn (Grid II), after correcting for area, the amount of scatter appeared to decrease (no figures are shown here), but for Sn-Cu (Grids I and III) no improvement was observed. Based upon the data and previous observations with extended plating time, it is suspected that in for the most part coverage is independent of the plating area. Another way to confirm this would be to plate on lithographically-masked wafers so that plating area variance is negligible.

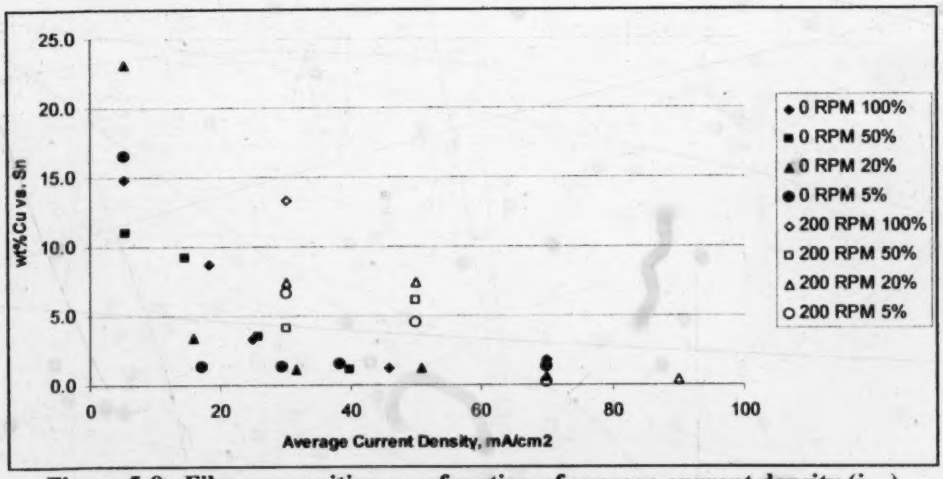

Figure 5-9– Film composition as a function of average current density (j_{avg}).

Film Composition for Deposits on Au-coated Substrates

Figure 5-9 shows the relationship between deposit composition and average current density. Overall, the amount of Cu present in the films seems to decrease with increasing j_{avg}. In addition, pulse duty seems to play a role at lower j_{avg} values, although the correlation is unclear. Above 50 mA/cm^2, only j_{avg} seems to have an influence. The data

point at 90 mA/cm^2 was measured to be 0.4±0.2wt%Cu, which is very close to the 0.7% target.

The trend is somewhat deceiving, since the variance at 5mA/cm^2 for an unagitated bath is between 11 and 23wt%Cu. Similarly, the largest variance for an agitated bath at 30 mA/cm^2 is between 4 and 13wt%Cu. Note that the EDX system uses flat standards for calibration, while the films plated at low j_{avg} tend to be rough. This may have an effect on the EDX composition values. Regardless, the percent Cu and level of variation seems to decrease with increasing j_{avg}. From a processing perspective, one may consider that plating at higher average current densities will yield less variation in film composition. Further, plating with unagitated baths yields near-eutectic films between 30 and 70 mA/cm^2.

Near-Optimized Plating on Au Substrates

If an eutectic (0.7wt%Cu) film is desired, then this becomes a very restrictive parameter. This is due to the fact that composition is a function of j_{avg}, but not pulse duty. Further, the unagitated bath chemistry used in this work yields a deposit with a minimum Cu content of 1.1wt%Cu. Agitation of the plating bath allowed for higher j_{avg} values, and a smooth film with 0.4±0.2wt%Cu was obtained.

For other film characteristics, there are similar restrictions. Good morphology is also confined to a narrow window of plating conditions; although the range of j_{avg} for a given pulse duty may be broader than that for composition. Coverage improves with decreasing pulse duty and increasing j_{avg}, so more flexibility is offered here. In the above cases, increasing j_{avg} seems to improve the deposit. Of course, there is an upper limit that has been observed as the critical current density or $j_{avg,c}$. Above this value, all deposits are highly dendritic. The $j_{avg,c}$ problem is also observed as edge dendrites, which form at lower j_{avg} value as a result of higher current densities at the edges of the plating mask.

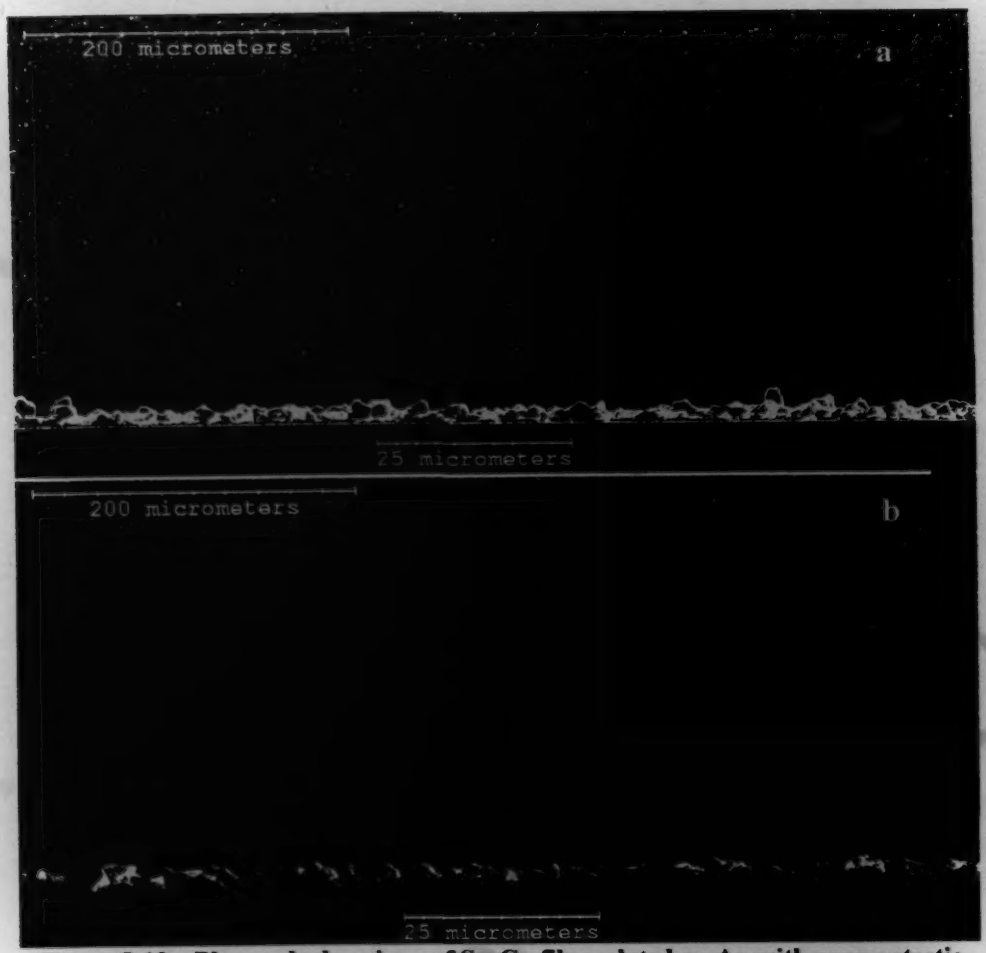

Figure 5-10 – Plan and edge views of Sn-Cu films plated on Au with near-eutectic (0.7wt%Cu) composition. Lighter shades on the plan view indicate higher regions on the film. (a) Film containing 0.4±0.2wt%Cu, plated at 90 mA/cm^2 with 20% pulse duty and an agitated (200 RPM stirring) bath. (b) Film containing 1.5±0.4wt%Cu, plated at 50 mA/cm^2, with 5% pulse duty and unagitated bath.

Note that other variables such as different levels of stirring should affect composition. These are not considered in this work. One might also expect Cu^{2+} concentration to be a factor. In an earlier investigation [Olsen 2004], however, solutions with a 20% higher Cu^{2+} concentration were used to deposit Sn-Cu films. The minimum attainable Cu content was similar to that for the current plating bath. This suggests that at such dilute Cu^{2+} concentrations, the reduction rate is no longer concentration-dependent.

Without any further optimization, the "best" film deposited on Au, whose composition was closest to 0.7%Cu appeared on Grid III as sample C6 in Figure 5-6 (i.e., 90 mA/cm^2 with p = 20% and 200 RPM stirring). A close-up is shown in Figure 5-10a. Unfortunately, low-Cu films such as C6 suffer from increased roughness. For comparison, a smoother film is shown in Figure 5-10b. This photo is a close-up of sample A9 from Grid I (Figure 5-4), plated at 50 mA/cm^2 with p = 5% and no stirring. The Cu content is 1.5wt%. For both films, however, edge dendrites are expected to be a problem. Note that films which are deposited using stirred plating bath tend to produce smoother films, but this is only at similar average current densities. In the above case, average current density was maximized in order to minimize Cu content. Stated another way, surface roughness seems to be a function of Cu content, with Cu-rich films being smoother. Of course, high-Cu films can be quite rough if j_{avg} is greater than j_{lim} for a given pulse duty.

Use of Citric Acid as a Stabilizer

Traditional acid-Sn plating baths use cresol sulfonic acid [Lowenheim 1978] to control oxidation of Sn^{2+} to Sn^{4+}. In this work, citric acid was investigated as a "green" substitute. Initially, low (up to 0.3 M) additions of citric acid produced films with promise. In all, four different variations on the standard solution were considered, as shown in Table 5-2. From each solution, a sample was plated, though in most cases the films were poor, with excessive numbers of dendrites.

Table 5-2 – Composition of solutions with higher acidity than the standardized solution

Solution	[H_2SO_4], M	[Citric Acid], M	[$SnSO_4$], M	[$CuSO_4 \cdot 5H_2O$], M
A	0.2	0.3	0.2	0.016
B	0.2	0.5		
C	0.2	1.7		
D	2.0	0		

Within a week, plating solutions containing H_2SO_4 turned yellow and became cloudy with yellow-white precipitates. With higher amounts of citric acid, the solutions

remained clear up to four weeks, but eventually yielded fine white precipitates that settled to the bottom of an otherwise clear solution. Finally, the solution would turn yellow and finally become cloudy. All solutions were stored in sealed glass flasks.

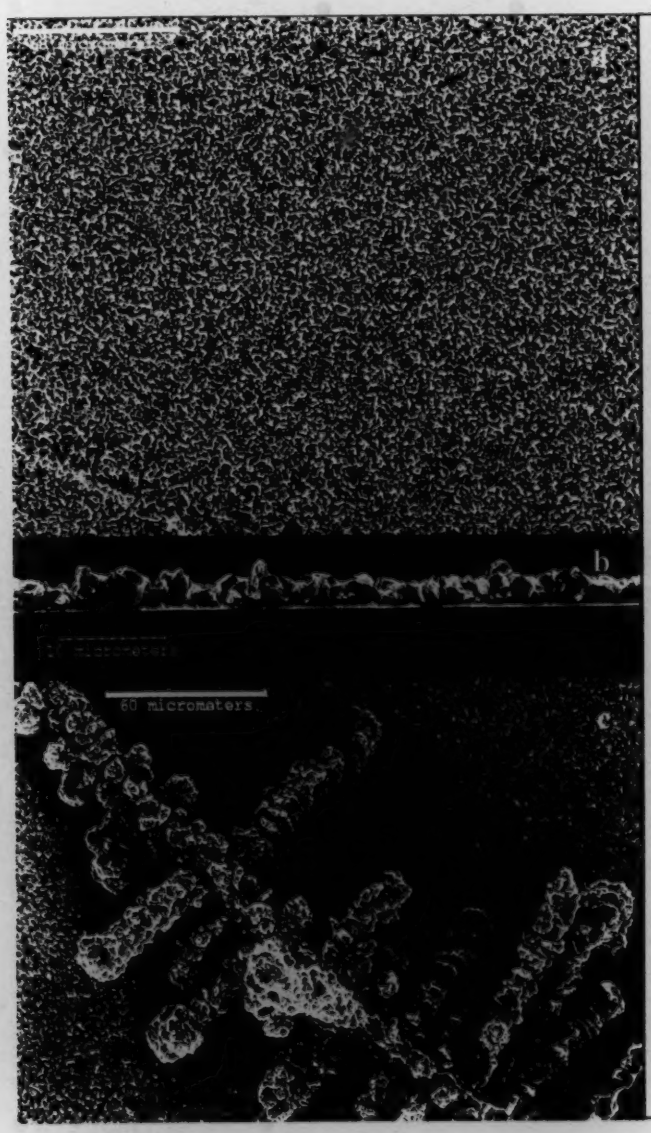

Figure 5-11 – Example of a near-eutectic (1.1wt%Cu) film plated on Au using citric acid.

a) Plan view showing good coverage (100%); 60 μm bar.

b) The film is somewhat rough, with a 0.6 μm/min plating rate that is typical of citric acid-free films plated at higher average current densities; 10μm bar.

c) Example of a dendritic defect that may be more common with citric acid additions; 60 μm bar.

Citric acid additions were found to affect the plating process in a number of ways. One benefit was that the anode surface did not foul. In addition, plated films contained less

Cu. Unfortunately, the limiting current density was severely reduced, and the appearance of dendrites on the surface of an otherwise smooth film was higher. No eutectic films were produced on Au using citric acid, although a 1.1wt%Cu film was produced on Au. The plating rate for this film was ~0.6 μm per minute, which is typical of some of the better films using the standard solution (Grids I and III). An example of a film plated with citric acid is shown in Figure 5-11.

It was found that citric acid enhanced the solution shelf life in proportion to its concentration. In this simple study, shelf life is defined as the ability of a solution to remain clear and colourless while stored within a stopped flask. Citric acid extended the standard solution shelf life from about one day to several weeks. In addition, one solution contained 2.0 M H_2SO_4 and no citric acid. It was found that the increased level of sulphuric acid enhanced shelf life, but not to the extent of citric acid.

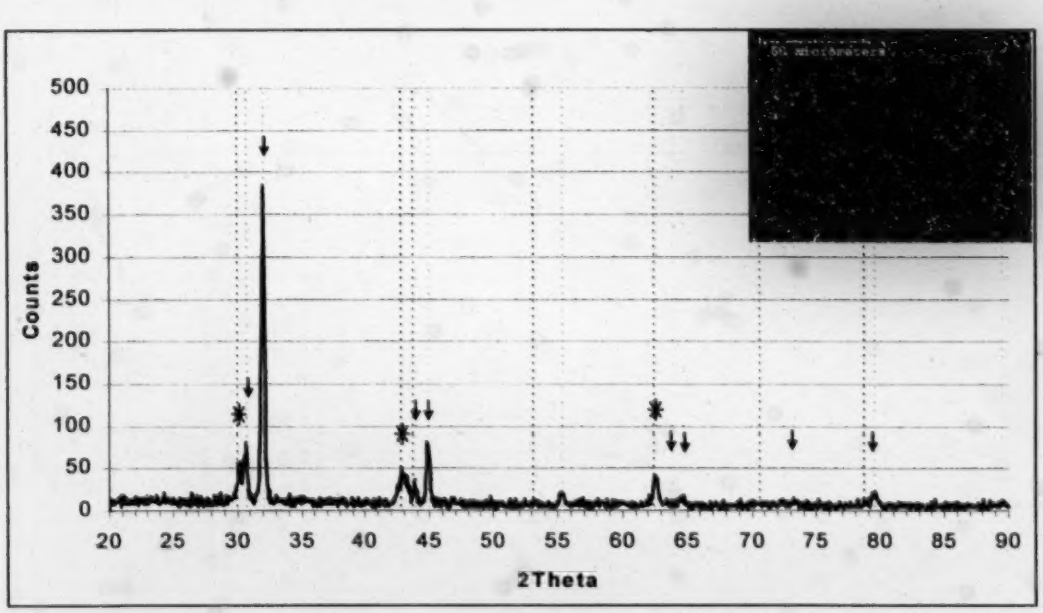

Figure 5-12- Sample plated at 20% duty. 10:1 Sn:Cu solution in 0.2 M H_2SO_4. 10 mA/cm^2 average current, 50mA/cm^2 peak current. (↓ = Sn phase, * = Cu_6Sn_5 phase, as determined from [Balikrisnan et al, 2003])

XRD Analysis and Aging of Additive-Free Baths

Sample spectra, from Sn-Cu deposits, are shown in Figures 5-12, 5-13 and 5-14 and show only Sn and Cu_6Sn_5 phases. No samples were measured with lower Cu contents, although one would not expect the Cu_3Sn phase (which is more Cu rich) to appear under such conditions.

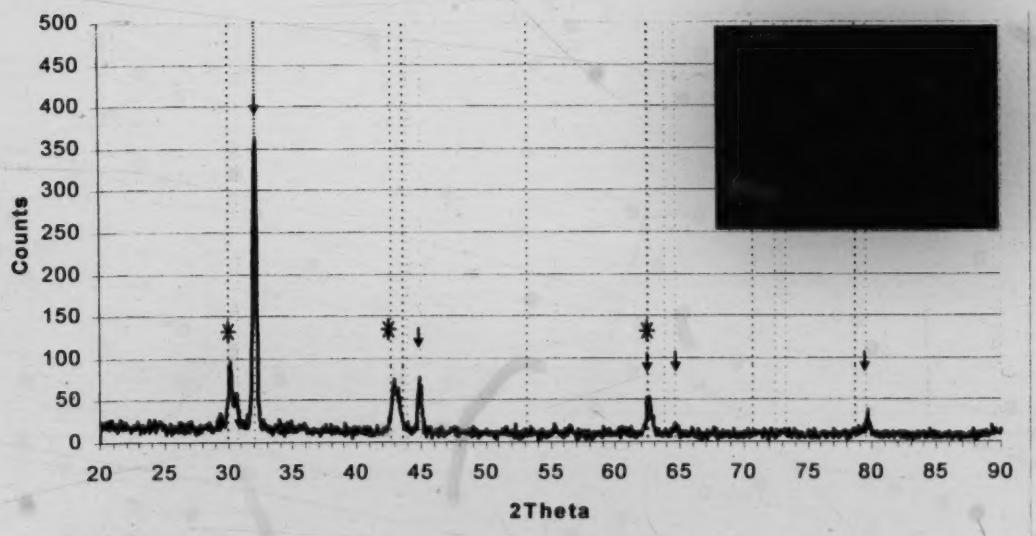

Figure 5-13 – Same conditions as Figure 5-12, but solution is 22 hours old with cloudy appearance. (↓ = Sn phase, * = Cu_6Sn_5 phase, as determined from [Balikrisnan et al, 2003])

The detectable phases were not observed to change, even though the overall Cu deposit concentration was measured to drop from ~22% to ~15% as soon as the solution became cloudy, even though there appears to be more Cu_6Sn_5 in the sample plated from a cloudy solution. Note that only the above two phases are expected, as illustrated in the Sn-Cu phase diagram of Figure 4-1, Chapter 4.

In the sample shown in Figure 5-14, the average current density (with fresh solution) was increased from 10 mA/cm^2 to 25 mA/cm^2. All the Sn peaks gave more counts, as

with the Cu_6Sn_5 peaks. Note that this sample has a higher Cu composition (31wt% versus 22wt% for Fig 5-12), as measured by EDX.

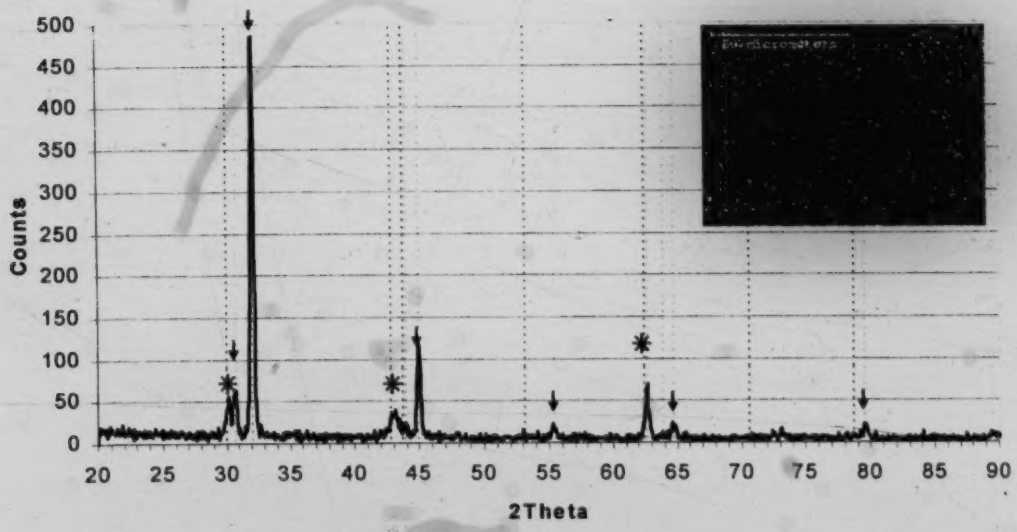

Figure 5-14- Sample plated at 20% duty. 10:1 Sn:Cu solution in 0.2 M H_2SO_4. 25 mA/cm^2 average current, 50mA/cm^2 peak current. (↓ = Sn phase, * = Cu_6Sn_5 phase, as determined from [Balikrisnan et al, 2003])

Conclusions

The influence of pulse plating on an additive-free Sn-Cu sulphate bath was investigated. It was shown that film morphology is greatly dependent upon pulse plating parameters. Film composition is also affected by pulse parameters, but the difference is only seen at low average current densities. Some of the films show promise, although there are a number of processing issues with an additive-free sulphate bath that probably cannot be overcome by pulse plating alone.

Table 5-3 presents an overall review of the films plated on Au substrates. It is based on the criteria listed in the beginning of the chapter.

Table 5-3 – Performance Review of Sn-Cu films

Criterion	Film Performance
Smooth, bright surface	Promising as a matte finish.
Resistance to edge effects	Poor. Edge effects are worse at higher average current densities, where near-eutectic film compositions are obtained.
Complete, consistent surface coverage	Promising. Complete coverage can be obtained if enough Sn-Cu is deposited. A relatively wide range of average current densities and pulse duty values yield acceptable coverage.
Eutectic composition	Eutectic compositions can be met using Au substrates.
Consistent composition	Au substrate samples were only analyzed in the middle of the plated area, so no conclusions can be made.
Resistance to whisker growth	Unknown at this time. Compressive stress was not measured, nor was a whisker test attempted.

Au-sputtered Si was a convenient substrate that allowed for fast quantification of coverage and composition of Sn and Sn-Cu films. A major drawback is the fact that no known industrial application would employ such a substrate. According to [iNEMI 2004-1], Sn-Cu is a solderable surface finish that is widely unpopular due to problems with whiskering of as-plated films.

The same study identified electroplated Sn on Ni as a popular solderable finish, however, and in the future this system could be studied in further detail. Recall that the incorporation of compressive film stress in the as-plated condition seems to be the culprit, and the presence of lower density Sn-Cu seems to make the problem worse.

As mentioned, a number of other applications exist for Sn-Cu that may warrant further investigation. To these ends, the additive-free PC plating process described in this chapter could be optimized. Examples are discussed in Chapter 7.

Chapter 6: Electrodeposition and Solderability of Sn-Cu Films on Cu Substrates

A version of this chapter has been published. K.P. Olsen and D.G. Ivey, "Solderability of Additive-Free, Pulse-Electrodeposited Sn-Cu Films," International Conference on Lead-free Soldering, May 2005, Toronto.

Introduction

The main purpose of this chapter is to evaluate the solderability of a Pb-free surface finish that was electroplated using an additive-free bath. This solderability study considers two Pb-free solders based on the Sn-Ag-Cu (or SAC) system.

The electrodeposition of Sn and Sn-Cu finishes on Cu substrates is seen as a possible industrial application. As such, some considerations were made regarding commercial potential and environmental compatibility. For example, the chemistry of the bath was kept as simple as possible, and the concentration of components relatively low. As previously mentioned, a sulphate system was chosen because of its simplicity, its popular historical use, its compatibility with both Sn and Cu systems, and finally because of its low cost. From an academic viewpoint, it is also of interest to see how far a simple, additive-free sulphate system can be stretched to yield acceptable Sn-Cu films.

From a processing perspective, an additive-free bath offers a number of perceived advantages. To begin, a small number of components should be easier to control. This is especially true considering that the breakdown products of typical Sn plating baths make in-situ measurement of additive levels very difficult [Tan 1993]. Secondly, neither the Sn nor Cu ions are complexed, which means

that spent solution can be reclaimed more easily [Muramatsu 2002]. In addition, a low-or-no additive solution will minimize entrainment of foreign material in the deposit. Finally, low levels of sulphuric acid and copper sulphate mean fewer operating and environmental hazards.

It should be noted however, that the Sn^{2+}/Cu^{2+} acid system is not very stable, with a shelf life that is less than one day. Over time, the Sn^{2+} quickly oxidizes to its Sn^{4+} state [Lowenheim 1978], and Sn precipitates begin to form. In this respect, at least one additive will eventually be required as an antioxidant if this electroplating system is to have any commercial viability. In addition, Pt anodes would be expensive, and the use of pure Sn or Sn-Cu anodes may need to be considered at a future time.

In addition to poor shelf life, the low-or-no additive criterion complicates the goal of plating a smooth, continuous film. Additives are typically used to control dendritic film morphology by suppressing the growth of existing nuclei in the deposit and enhancing the formation of new ones. From previous plating work, Sn was observed to be an especially difficult metal to plate; crystal growth tends to dominate nucleation, and a rough deposit results. According to the literature [Tan 1993], [Lowenheim 1978], [Price 1983], common additives for morphology control of Sn include gelatin and β-napthol. The β-napthol (a hazardous additive) is required to control dendritic morphology, while the non-hazardous gelatin is used to enhance the solubility of the β-napthol in sulphuric acid solution.

A newer, albeit well-investigated approach to emulating the morphological effects of additives is the use of a pulsed current or voltage [e.g., Puippe 1986-1] during deposition. Figure 6-1 shows that for a set average current density output (j_{avg}) one can choose a variety of different waveforms. Each is able to change the behaviour of nucleation and growth during electrodeposition of a film. A more complete description of pulse plating is given in Chapter 4.

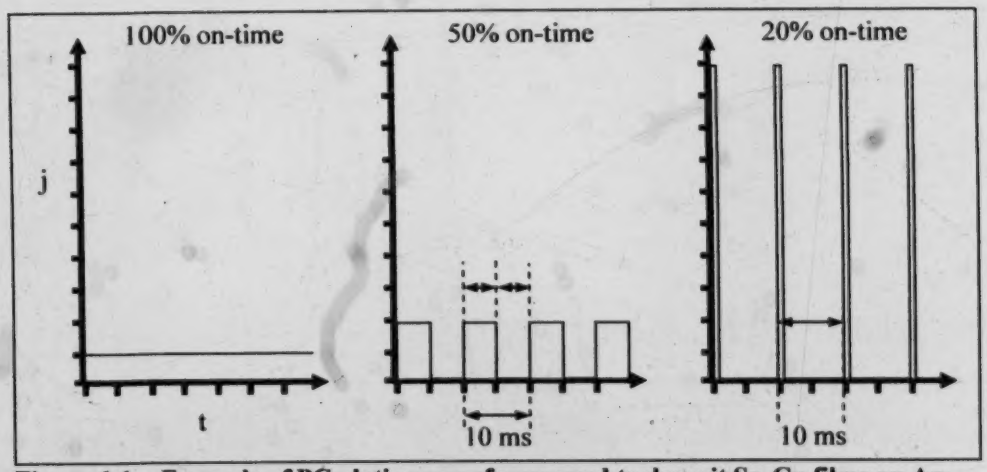

Figure 6-1 – Example of PC plating waveforms used to deposit Sn-Cu films on Au and Cu. All three waveforms have the same average current density.

During deposition of a pure material (Sn, for instance), one may consider a model [Bard & Faulkner 2001], [Puippe 1986-1] wherein the cations in an electrolytic cell are drawn to the cathode and reduced to a neutral charge. The motion towards the cathode is a result of migration (electrostatic attraction), diffusion (due to a concentration gradient), and forced convection (due to electrolyte agitation). Regardless of the mechanism, these surface cations may be thought of as adatoms which add mass to the cathode deposit by either nucleating new crystals or attaching themselves to existing ones.

Crystal nucleation and growth are competing processes [Puippe 1986-1]. Nucleation is favoured with high adatom concentration, low mobility and high overpotential. On the other hand, growth is favoured at low adatom concentration, high mobility and low overpotential. For a system with fixed composition and concentration, overpotential is the defining parameter.

In this work, a simple square wave current pulse was modified so that the overpotential was either high (low pulse duty) or low (high pulse duty), as described in previous chapters.

Note that the original work on this sulphate system dealt with the deposition of Sn-Cu deposits on Au-coated Si wafer substrates (Chapter 5). These were a convenient choice for a number of reasons:

1. Si wafers cleave easily. Cross-sections of Sn-Cu films can therefore be readily obtained.
2. During examination by optical microscopy and SEM, the Sn-Cu deposits can easily be differentiated from the substrate. The composition of poorly-covered films can be measured using EDX analysis, and the covering power of a particular set of plating conditions can similarly be quantified by measuring the total Sn + Cu content versus Au.

Such a luxury was not possible with ~1 mm thick copper substrates. As a result, composition values of thinner films may be influenced by the substrate and the samples had to be mounted and polished using a metallographic procedure described later in this chapter.

In the absence of additives, it was demonstrated in Chapter 5 that a pulsed current could be used to obtain a wide range of film compositions and morphologies. The data gathered from the Au substrate work was used to develop a pulse-plating procedure for Sn-Cu films on Cu, as described below.

Experimental Procedure

Cu Substrate (Cathode) Preparation for Electrodeposition Work

The Cu substrates were cleaned using the technique listed below. In both cases, the purpose was to remove oils and/or surface oxide from the surface of the copper. The substrates were sheared from wrought Cu sheet to approximately 1 cm by 2.5 cm. Originally some commercial Cu cleaner had been ordered from Cookson Electronics. The company no longer sells this product, however.

- Submerge in near-boiling water with Sparkleen® detergent for under 10minutes.
- Rinse three times using distilled water.
- Submerge in isopropyl alcohol for one day.
- Dry on paper towel.

After private communications with sales staff from Cookson Electronics, it was decided that a more aggressive cleaning technique be used, and an attempt should be made at removing the surface oxide. The use of hot water tended to tarnish the copper pieces. The use of 600 grit paper turned a near-mirror-smooth finish to a "brushed" look. Under an optical microscope, no evidence of embedded grit was observed within the sanded Cu, although the increased roughness was quite apparent.

Most of the other preparation steps were the same as for Au, as described in Chapter 5. This includes surface marking and masking. Pt-coated Si anodes were also used, and placed 2.0 cm apart. The anode to cathode ratios varied, but as before the anode area was equal to or greater than the cathode area. With the pure Cu substrates, the sides and back of the sample must be coated with lacquer. Sometimes a second coat of lacquer had to be applied along the edges because bare spots would form during drying.

In addition, mirror-smooth Cu substrates were prepared by sputtering a ~250 nm layer of Cu on a Ti-coated Si wafer. The Ti was sputtered to a thickness of ~25 nm and served as an adhesion layer.

Cu Substrate (Cathode) Preparation for Solderability Trials

A second set of Cu substrates was also made from shearing 1 cm by 2.5 cm pieces of 1 mm thick Cu sheet. Surface oxide was removed by washing for 30 s in 2 M H_2SO_4. Next, they were washed in a dilute solution of residue-free

detergent, then rinsed three times with distilled water and finally rinsed in isopropyl alcohol.

After cleaning, the surfaces of all samples were bright and relatively smooth and ready for masking. Most samples contained a few scratches from fabrication and handling. A 5 mm by 5 mm area was marked off at the corners using a fine-tipped felt marker, and lacquer was manually applied to serve as a plating mask outside of the marked area which was left overnight to dry. The actual plating area dimensions varied between 4 and 6 mm in width and height. Due to the manual application, the plating areas were not perfectly square. The actual width and height were measured to the nearest 0.25 mm and the calculated area was used to determine the output of the pulse plating power supply.

For electroplating, a solution consisting of 0.2 M H_2SO_4, 0.2M $SnSO_4$ and 0.016 M $CuSO_4 \cdot 5H_2O$ was made in 250 ml batches using the same techniques outlined in Chapter 5. For each electroplating experiment, about 60ml of solution was added to a 250 ml beaker, with machined polypropylene electrode holders.

Initially, a procedure based on the Au substrate work was used for deposition on the pure Cu substrates. A high average current density was used in order to keep the Cu content to a minimum, and also to maximize the rate of deposition. The results were quite poor, however. During plating, a large area of the Cu evolved gas bubbles (presumably hydrogen). These bubbles tended to stick to the Cu, thereby restricting electrodeposition. On the bubble-free regions, Sn-Cu was deposited, but it was a rough mass of highly dendritic growths.

To determine whether this was a material issue, some of the Cu-coated Si wafer samples were also plated using the same "best" electroplating procedures for Au-coated Si substrates. Once again, poor results were obtained.

Eventually, a two-step process was devised for depositing Sn-Cu on pure Cu using a single bath. A high-Cu "base" layer (or "strike") was first deposited using a low average current density (j_{avg}). Following deposition of the base layer, a low-Cu "cap" layer was deposited using a much higher j_{avg}. The two-step method yielded a relatively smooth, bubble-free film with generally good coverage. However, the EDX-measured Cu content was about 3wt%, and a large number of dendrites were observed to form around the edge of the film. Note that Sn-0.7wt%Cu (eutectic) has the lowest melting point.

During the two-step process, the electroplating solution was stirred at the center of the beaker using a glass impellor rotating at 200 RPM. A new anode, made of a Si wafer coated on one side with Pt, was used for each deposition. The distance between the anode and cathode was fixed at about 2 cm. The anode-to-cathode area ratio varied somewhat, but was approximately 1:1 or higher.

Before plating, the pulse-plating power supply used for the work in Chapter 5 was programmed and the output confirmed using an oscilloscope. Then a base layer was pulse-plated at j_{avg} = 25 mA/cm^2 and p = 5% with a 2.5 mA/cm^2 reverse pulse lasting 0.5 ms over a repeating 10 ms cycle until 60 mA*min of charge was transferred (about 10 minutes plating time). The reverse pulse was used to lower the rate of dendritic growth around the edges of the plating area. Finally, a cap layer was pulse-plated at j_{avg} = 70 mA/cm^2 and p = 20% until 140 mA*min of charge was transferred (about 7 minutes).

After plating, the sample surface was rinsed using distilled water and then removed from the polypropylene electrode holder. The water rinse removed most loose deposits of Sn-Cu from the edge of the sample. The red lacquer plating mask was dissolved away in acetone. Approximately 30 samples were plated for use in the solderability trials. As a final step, dendrites that still remained on the edges were carefully removed.

Solderability Test Procedure

Two types of solder were used to test for solderability using a dip-and-look test. The first was a SAC solder containing 96.5wt%Sn, 3wt%Ag and 0.5wt%Cu. The second was a SAC-X solder containing 98.9wt%Sn, 0.3wt%Ag, 0.7wt%Cu and 0.1wt%Bi. Each solder was melted at about 260°C during one series of trials. The SAC solder was also heated to 276°C during a second series of trials. Plated samples were dipped in an RMA flux containing 25% solids. The samples were held just above the molten solder for up to 10 seconds, then slowly dipped into the molten solder, submerged for 5 or 10 seconds and slowly withdrawn.

Before dipping in solder, four samples were pre-oxidized by heating in air to 100°C for 1 hour. An additional four samples were oxidized in this way, and then also oxidized by steam exposure for 3 hours. During steaming, the Cu samples were placed in a plastic holder, and standard ANSI/J-STD-002 steaming specifications were followed except for three conditions. First of all, the Sn-Cu surfaces were less than the 38 mm minimum recommended distance from the hot water. Secondly, the water was heated to boiling, rather than to 7°C below the local boiling point. Thirdly, the samples were air dried at 100 °C for 10 minutes (rather than at ambient temperature). The pre-oxidized samples were dip tested in SAC solder only.

Metallographic Preparation

Samples were cold mounted using a polymer with a cure temperature below 30 °C. This was done to preserve the as-plated structure of the Sn and Sn-Cu. All grinding and polishing steps were carried out using an automatic polisher. In order to analyze the middle of the Sn-Cu film area, about 3 mm from the bottom edge was ground away using 320-grit SiC paper. During the final stages of grinding, wax was added to the paper to minimize the embedding of SiC particles into the soft Sn. Subsequent grinding steps used 600 and 800-grit paper with wax.

Polishing was done with 1μm unagglomerated alumina and finally 0.05 μm alumina.

Results and Discussion

Sn-Cu Electrodeposition on Cu and Cu/Si Substrates

Recall that initially, conditions that yielded good films on Au were used to plate Sn-Cu on rolled Cu substrates and all attempts resulted in poor films with the co-production of bubbles on the cathode. A short study was carried out on Cu-sputtered Si to determine if the problem was due to the change in material (i.e., Au to Cu) or the increased surface roughness of the rolled Cu. In the end it was determined that both substrate composition and surface roughness played a role, although the material change had the greatest impact.

Table 6-1, Examples of Extended Plating Trials

Sample	j_{app} mA/cm²	Pulse Conditions	Comments
Cu2-1	FWD = 50	200 RPM agitation FWD 0.5 ms on, 9.5ms off	"Best" conditions on Au (Grid III, with agitation). Poor film with dendrites.
Cu2-3	FWD = 50 REV = 5	200 RPM agitation FWD 0.5 ms on, 8.5 ms off REV 0.5 ms on, 0.5 ms off	Same as Cu2-1, but with 10% reverse pulse to control edge dendrites. Good film. 7.1wt%Cu±0.6
Cu2-4	FWD = 60 REV = 6	200 RPM agitation FWD 0.5 ms on, 8.5 ms off REV 0.5 ms on, 0.5 ms off	Same as Cu2-3, but slightly higher current density. Poor film with dendrites.

The question still remains as to why there was such a difference in film morphologies when switching from a sputtered Au to a wrought Cu substrate. It is known that the hydrogen evolution reaction (HER) overpotential can vary depending upon the composition of the cathode [Bard & Faulkner 2001]. The work of [Trasati 1972] was consulted in order to gauge the relative difference between Cu and Au. However, the data for hydrogen reduction in 0.5 M H_2SO_4

solution shows that the exchange density for hydrogen reduction on Au is one-to-two orders of magnitude larger than Cu, which suggests that the HER overpotential for Au should be less than Cu.

In an attempt to improve the films, a number of other conditions were tried. Table 6-1 gives a partial list, along with EDX measurement of composition. An example of a plated layer with defects is shown in Figure 6-2. Such films exhibited spots with poor coverage, which is attributed to incomplete surface cleaning. In nearly every other plating sample, the film was thinnest at its center. The defect in Figure 6-2 is off-center, suggesting that a reason other than electric field variation is to blame. One possibility is residual dirt or oxide on the surface of the copper. Figure 6-3 shows plan and edge views of the strike layer alone and a strike layer that has been capped. Examples of poor films plated under non-ideal conditions are shown in Figure 6-4. Samples were also plated on a Cu surface roughened using 600 grit SiC paper, and poorer films were obtained.

Figure 6-2 – Views of the best film on Cu at various magnifications (Sample Cu2-3). There is a single region of poor coverage in the top image marked by an arrow. All other areas are completely covered. Typically, areas of poor coverage are at the center of the plated area, suggesting that this may possibly be due to poor surface preparation.

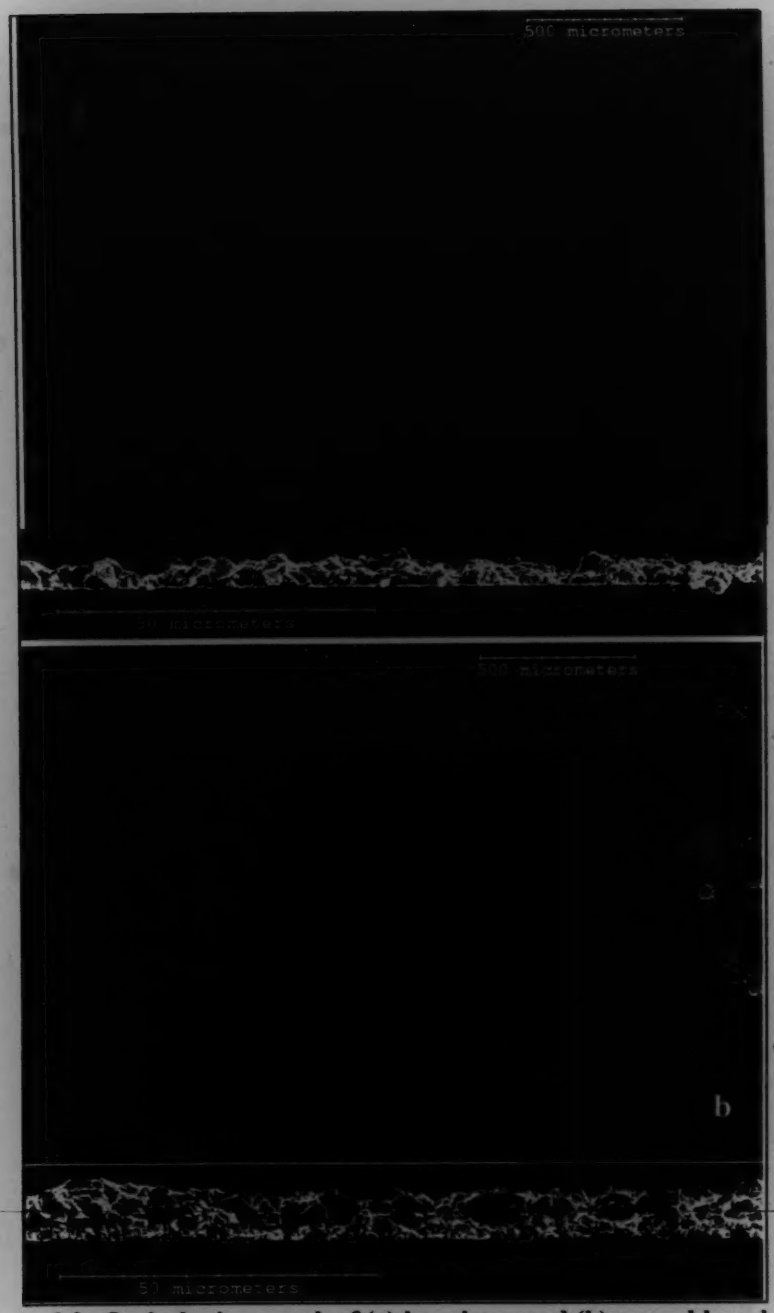

Figure 6-3– Optical micrograph of (a) base layer and (b) capped base layer. Most of the edge dendrites were removed after plating and rinsing.

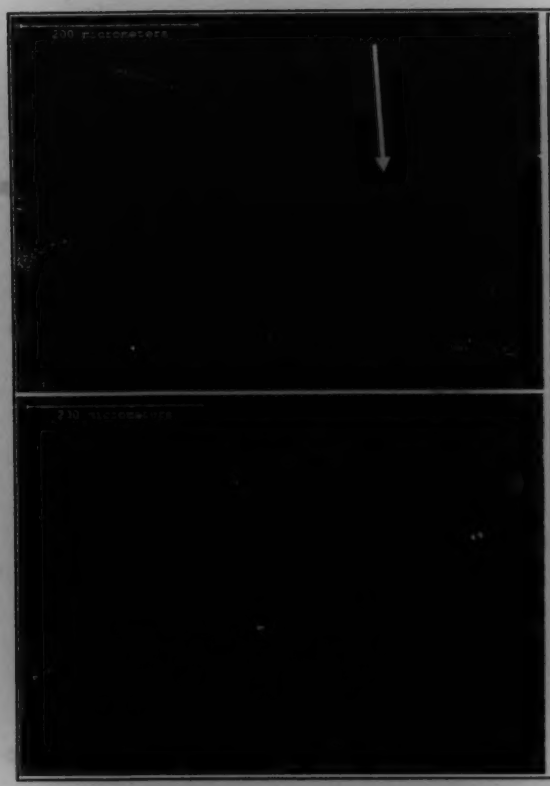

Figure 6-4– Plan views of sample Cu2-1 (top) showing a possible site on the right-hand side for hydrogen formation (arrow) and sample Cu2-2 (bottom). These are typical of the poor deposits outlined in Table 3-1.

Edge dendrites are a problem that seems difficult to solve through the exclusive use of pulse plating. During deposition on Cu, a reverse pulse was added to each cycle. The duration was similar to the forward pulse, but the magnitude of the current density was set at 10% of the forward value. This seemed to have a small effect on edge dendrite growth, while increasing the time required for plating. It is understood that the formation of dendrites will increase the surface area of the cathode, and therefore reduce the effective average current density. This should increase the Cu content of the film. Further work is required to reduce edge dendrite formation, and through the reduction in cathode area over time it is expected that such efforts will therefore reduce the Cu content as well.

A photo of an unoxidized and a preoxidized sample is shown in Figure 6-5. Recall that while most of the edge dendrites were removed by the final rinse step, some had to be scraped away.

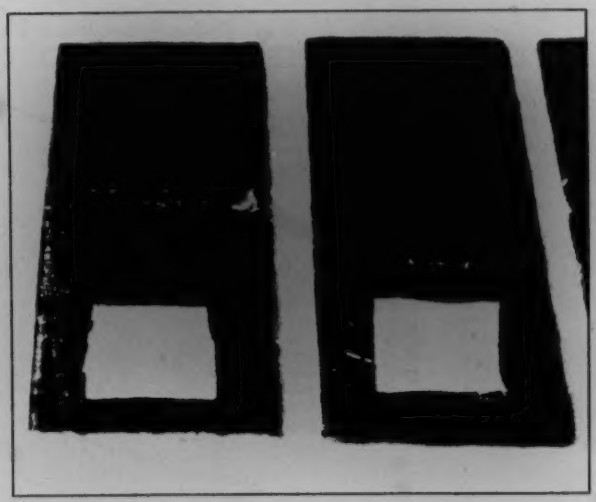

Figure 6-5– Cu samples plated with Sn-Cu film measuring about 5 x 5mm. The sample on the left is as-plated. The sample on the right has been oxidized by heating in air at 100°C for 1hr, and then exposed to steam for 3hr.

Solderability Work

As-soldered samples were examined visually using two criteria. The first was evidence of a continuous covering of solder over the sample surface. The second was evidence of a reduced wetting angle as compared with the bare Cu. The best sample from each trial is shown in Figures 6-6 and 6-7. An average of four samples was used for each set of conditions. The use of the best samples for analysis is justified by considering the fact that successful soldering is dependent upon a number of carefully-controlled parameters. Since the soldering method used in this study was not optimized, the best sample from each set of conditions was deemed to occur when "everything went right." In a future study, the procedure should be optimized and should also conform more closely to the ANSI/J-STD-002 standard. In addition, a scientist from Research In Motion has offered to do more quantitative testing work using a wetting balance. This is discussed further in Chapter 7.

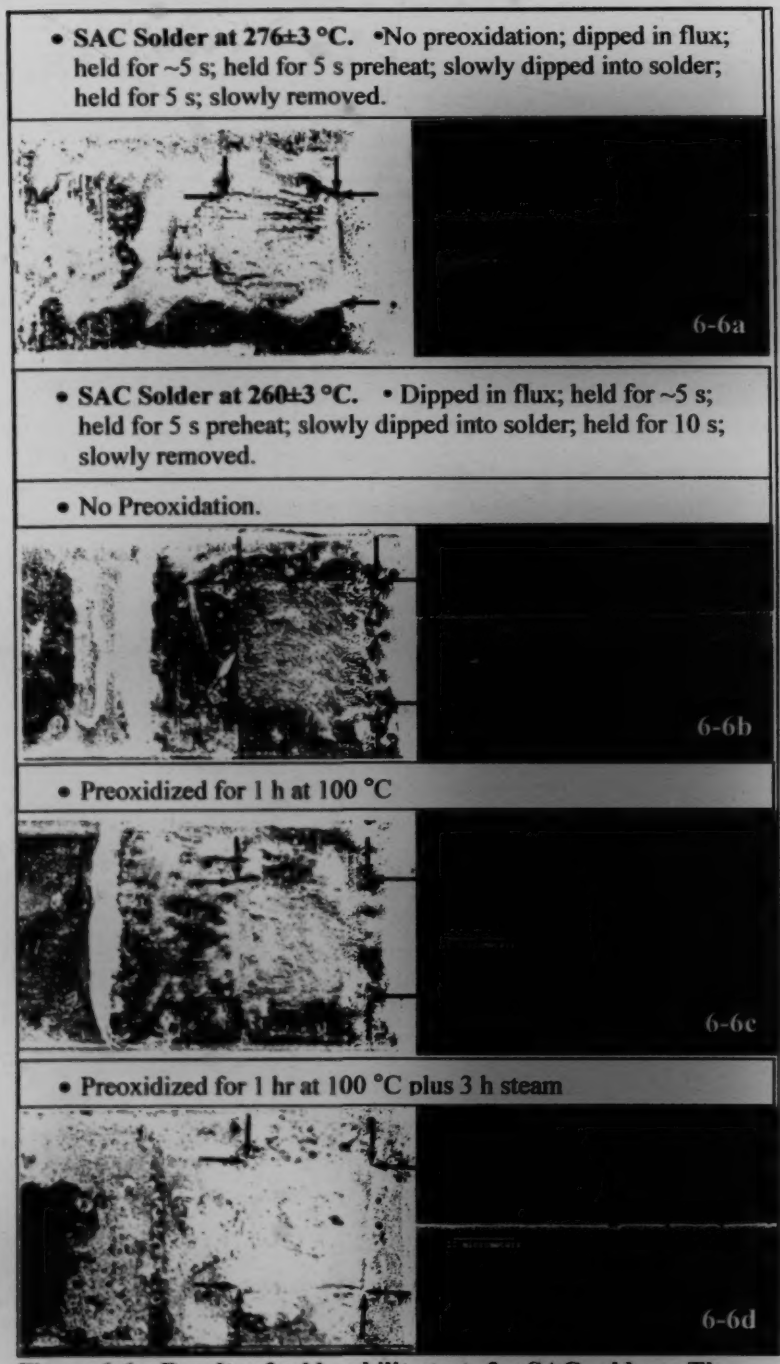
• SAC Solder at 276±3 °C. •No preoxidation; dipped in flux; held for ~5 s; held for 5 s preheat; slowly dipped into solder; held for 5 s; slowly removed.
6-6a
• SAC Solder at 260±3 °C. • Dipped in flux; held for ~5 s; held for 5 s preheat; slowly dipped into solder; held for 10 s; slowly removed.
• No Preoxidation.
6-6b
• Preoxidized for 1 h at 100 °C
6-6c
• Preoxidized for 1 hr at 100 °C plus 3 h steam
6-6d

Figure 6-6 – Results of solderability tests for SAC solders. The plated areas (underneath a layer of solder) are marked with arrows.

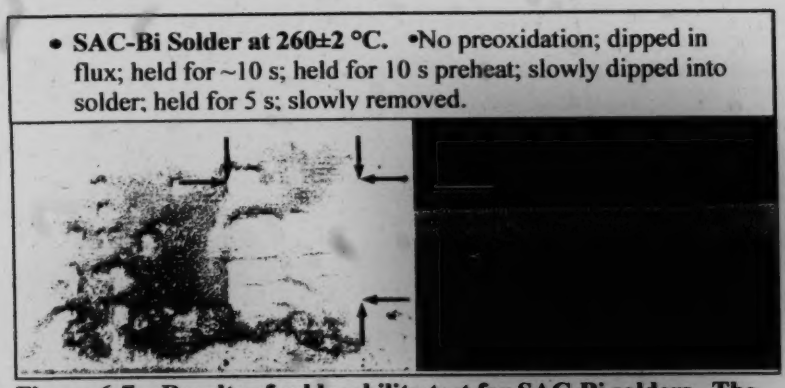
• SAC-Bi Solder at 260±2 °C. •No preoxidation; dipped in flux; held for ~10 s; held for 10 s preheat; slowly dipped into solder; held for 5 s; slowly removed.

Figure 6-7 – Results of solderability test for SAC-Bi solders. The plated areas (underneath a layer of solder) are marked with arrows.

The first criterion (good coverage) was met for all but sample marked 6-6d in Figure 6-6. Well covered films were observed to have a thin, relatively smooth covering of solder over the plated Sn-Cu. For the SAC-soldered samples, it is possible to clearly see the Sn-Cu film edges. Sample 6-6d represents the heavily oxidized samples (heated air + steam). Poor solder coverage is seen as pinholes on the square Sn-Cu area. The situation is worse on the bare Cu surface, however. Note also that there are dark spots visible near the arrows on all the samples in Figures 6-6 and 6-7. These are a result of the felt marks used during masking, which seem to function as a non-wettable surface.

The second criterion (lower wetting angle vs. bare Cu) was also observed, in that the solder coating is quite bumpy on the bare Cu surface surrounding the Sn-Cu film. The difference in flatness is attributed to a difference in wetting angle. None of the Sn-Cu films have a completely flat covering of solder over their entire area. Unfortunately, it is difficult to determine the reason for this. One possible explanation is that excess solder, balled up on the bare Cu surface would have been the last to solidify. During withdrawal from the solder pot, some of the solder could have spilled onto the solidified solder layer on the Sn-Cu film.

During analysis of the cross-section micrographs, a well-bonded Sn-rich layer was observed over the Cu. In Figure 6-6, one can see a general thinning trend with increased oxidation. Given the large variance in thickness for most samples, it is difficult to tell whether the trend is real. All but a few areas of un-plated Cu were covered as well, however. The film thickness seemed quite variable over the entire sample area, ranging from only a few microns to 10 μm or more. The porosity seen in the Sn-alloy (lighter layer on top of the darker Cu) is considered to be shrinkage voids. A second possibility is Kirkendall voids, although this is much less likely since any Kirkendall void formation is a solid-state diffusion phenomenon. After soldering the sample would have cooled rapidly, thereby minimizing solid-state diffusion.

For the SAC samples, the largest difference in wetting angle between wetted Cu and wetted Sn-Cu was observed in the sample marked 6-6a (Figure 6-6). Here, a much higher solder pot temperature was used, and the sample was preheated for only 5 seconds.

Overall, the SAC solder seems to exhibit a lower wetting angle on Sn-Cu versus bare Cu. With the SAC-X solder, this distinction is much less clear. For both solders, the angle of the liquid solder meniscus against the Cu sample was observed to change from unwetted to wetted after about 3 seconds of immersion.

During SEM analysis, the amount of Ag was measured using EDX on two cross-sections. It was found that a relatively constant level of Ag was detected throughout the entire Sn-rich layer. This suggests that a large amount of plated Sn-Cu is being dissolved during the soldering operation.

As a final caveat, it should be noted that for each set of conditions at least one sample showed almost no evidence of a reduced wetting angle. In a future series of tests, it may be beneficial to coat the bare Cu surface with a solder resist. In

this way, the solderability of only the Sn-Cu film can be gauged. Figure 6-8 shows a cross-section with variances in solder wetting angle. Note that only the top surface was plated with Sn-Cu, while the bottom surface was bare Cu.

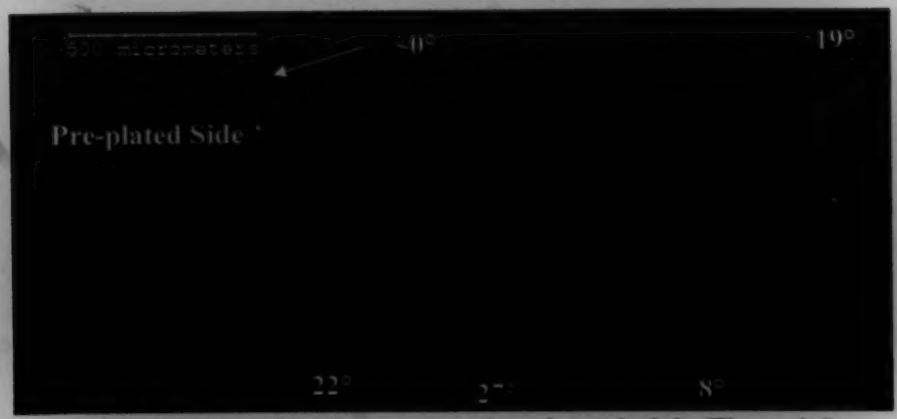

Figure 6-8– Low-magnification cross-section of sample 6-6a (Figure 6-6). The top (pre-plated) side is covered with a thicker and more continuous layer of Sn alloy than the bottom (unplated) side. On both sides, there is evidence of zero degree wetting layers (e.g., top left) and various other wetting angles.

Summary and Conclusions

An additive-free approach has been employed to deposit relatively smooth films of near-eutectic Sn-Cu. The purpose of the Sn-Cu is to protect a pure Cu surface and also to enhance its solderability. While the un-optimized procedure holds promise, there are a number of outstanding issues with respect to bath stability, maintaining consistent morphology at the film edges and a minimum 3wt%Cu film composition.

A continuous layer of solder was observed over the plated Cu for un-oxidized and mildly oxidized samples. There was evidence of a smaller wetting angle over the plated areas, relative to the bare Cu surfaces. The most severely oxidized samples exhibited some dewetting on the plated Cu area, but they still fared better than bare Cu.

Optimization of the Sn-Cu plating procedure must include a way to reduce dendritic growth on the edges. From the solderability tests, the higher Cu content may not be a problem. However, the solderability tests themselves should be optimized and follow the ANSI/J-STD-002 standard more closely. The use of a solder resist over the bare Cu would help analysis of the plated surfaces.

Overall, the outlined procedure for Sn-Cu plating on Cu may hold promise as a commercially-viable, solderable film that offers protection from oxidation.

Chapter 7: Final Considerations and Future Work

Introduction

The purpose of this chapter is to consider the opportunities for future development of the Sn-Cu sulphate bath for commercial applications. A summary of issues that may be addressed for the deposition on Au, Cu and solderability of plated Cu is given below. In the following section, a number of these topics are discussed in further detail.

Work presented in Chapter 5 summarized the use of square waveform pulses as a means of simulating additives for Sn and Sn-Cu sulphate baths. It was shown that film morphology was greatly influenced by variations in pulse duty over a 10ms cycle. Film composition was much less influenced by pulse duty. Rather, both current density (at values high enough to yield smooth films) and agitation were defining parameters. One example includes varying pulse parameters such as the 10ms cycle length or elimination of zero current during off time. In addition, a number of strategies could be explored in an effort to enhance solution stability (i.e., shelf life) and switching from expensive Pt anodes to consumable Sn or Sn-Cu.

In Chapter 6, solderability trials were performed on films plated with an un-optimized procedure. An example of optimization work includes a means of minimizing edge dendrite formation while plating low-Cu films (~1wt%Cu) on Cu substrates. Note that the strike layer is deposited much more slowly than the cap, so there is room to increase the overall plating speed *and* lower Cu content by minimizing the thickness requirement of a well-covered strike. In addition,

there is an opportunity to do extended solderability work with an industrial partner.

It would also be of interest to repeat some plating experiments using patterned cathodes in order to see if the level of scatter in coverage and composition data can be improved. Plating on patterned substrates would also allow the evaluation of Sn-Cu for Level I applications.

Finally, concerns with whisker formation may be addressed. In this case, whiskers are defined as spontaneous rod-like growths of single-crystal Sn measuring up to several millimeters in length [e.g., Zeng & Tu 2002].

Future Work

Electroplating Bath Development

Relatively constant compositions (1.5wt% Cu) versus j_{avg} were observed for unagitated films on Au substrates. Lower Cu contents are possible, and a similar leveling of composition was seen to occur at higher j_{avg} values for agitated films, though the range of densities was much narrower. From the literature presented in this thesis, a composition of up to 1.5wt% seems acceptable for use as a solderable finish. In addition, solderability work presented in Chapter 6 showed that even larger (3 to 5wt%Cu) contents hold promise.

Table 7-1 outlines a number of issues with the current setup. It summarizes some possible solutions as well. For example, an important issue with the Sn-Cu (or Sn) electroplating bath is solution stability [e.g., Swanson & Zhang 2002]. While ultimately an additive will be required for shelf life, replacing the Pt anode with a consumable one may improve stability during operation simply by eliminating the oxygen-forming oxidation reaction. According to [Zhang & Abys 2000], electroplating Sn in a methane-sulphonic acid solution further increases stability

and impedes oxygen formation at the anode. The same solution allows for higher current densities which equates to higher plating rates. This is because the solubility limit of Sn is much higher.

It should be noted that the concentration of $SnSO_4$ was increased by 50% and 100% (from 0.2 M) in a small number of experiments. Plating conditions that yielded good films for the standardized solution were employed. In all cases, a sparse deposit was plated that looked similar to the low j_{avg} (5-15mA/cm^2) films. The appeal of higher Sn concentrations is higher plating rates [Lowenheim 1978]. In addition, it would mean a higher Sn^{2+}:Cu^{2+} ratio, which could allow eutectic films to be plated over a wider range of average current densities. Recall from Chapter 5 that the Cu^{2+} concentration was reduced from 0.002 M (preliminary work) to 0.0016 M (thesis work), without any significant drop in minimum film concentration.

Table 7-1 – Process Issues with Pulse Plating of a Sn-Cu Sulphate Bath

Process	Problem	Description	Possible Solutions
Anodic	Oxygen formation at anode	▪ Presence of oxygen accelerates the oxidation of $Sn^{2+} \rightarrow Sn^{4+}$ [Tan 1993]	▪ Use soluble (Sn) anode to eliminate oxygen formation. ▪ Change to methane-sulphonic acid.
	H^+ formation at anode	▪ H^+ formation leads to a localized pH drop and corresponding solubility drop of $SnSO_4$. The salt precipitates on the anode, causing passivation. [Zhang & Abys 2000]	
Cathodic	Pronounced edge effects	▪ Very large dendrites grow on the edges.	▪ Add organics to reduce deposition on high energy sites. ▪ Vary the reverse pulse parameters.
	Sulphur in deposits	▪ Sometimes small amounts of sulphur are detected on Sn-Cu films plated at high j_{avg}.	▪ Requires more investigation.

While there are some perceived advantages of using an additive-free electroplating bath with pulsed deposition, the technique is not yet optimized. In addition to the stability issue, Cu immersion plating is known to occur when zero current is applied, and this may necessitate the use of additives [Khaselev et al 2002]. Table 7-1 summarizes the problems encountered from an experimental processing perspective. Also included are possible solutions. In a commercial process, Pt would likely need to be replaced with consumable Sn, Cu or Sn-Cu anodes because of cost.

Recall that a new Pt-coated anode was used for each plating experiment. The reason for this was that the surface would become "fouled" with a light, powdery film. [Zhang & Abys 2000] attribute this problem to H^+ formation at the anode, which causes a pH drop and therefore a drop in the solubility limit of $SnSO_4$. The film is therefore thought to be $SnSO_4$, and it was difficult to clean. Note, however, that the Pt anodes in solutions containing citric acid did not foul.

There is much work in the literature concerning the use of additives [Muramastu 2002], [Fukuda et al 2002], [M. Fukuda et al 2003-1], [Survial et al 1997], [Stoychev & Tsvetanov 1995], [Fabricius et al 1995], [Brown & Hope 1995], [Brown et al 1994], [Lin et al 1996], [Nakamura et al 1994-1], [Nakamura et al 1994-2], [Galdikiené & Mockus 1994], [Urda et al 1996], [Urda & Oniciu 1996], [Kaneko & Nezu 1989], [Carlos et al 2000], [Tzeng et al 1995], [Farndon et al 1995], [Stanković and Vuković 1996]. In some cases, such additives may be employed (with pulse plating) to improve film properties and reduce the tendency to form dendrites along the edge. Note, however, that some insights may be gained by plating on patterned cathodes with thin and consistent mask edging, although the dendrite problem seems to be a feature of pulse plating itself [Kim & Ritzdorf 2004]. The above-cited references are concerned with additives that either form complexes or serve to "poison" the high-energy or active growth sites

on the cathode. Examples of the later are polyethylene glycol (PEG), gelatin or thiourea, as suggested for use with Cu and Sn by [Brown & Hope 1995], [Brown et al 1995], [Stoychev & Tsvetanov 1995]. Note that non-complexing additives should allow for easier reclaiming of spent electrolyte, although one should expect entrainment of organics in the deposit.

An interesting additive is phosphoric acid (H_3PO_4), as described by [Urda & Oniciu 1997]. The authors suggest that additions of the acid to $CuSO_4 \cdot 5H_2O$ + H_2SO_4 could be used to replace more traditional additives (gelatin, thiourea and Cl^-) that require tight concentration controls in order to plate high-quality Cu films. Also, the addition of 1 g/*l* H_3PO_4 or more is shown to greatly increase the current density of Cu at a given potential. As such, the voltage requirement to deposit Cu at a prescribed current density would be shifted towards that of Sn. An appealing feature of H_3PO_4 is that it is present in food products. One would therefore expect it to be environmentally friendly and plentiful. It is not known how phosphoric acid would affect Sn, however.

Variable Cycle Length

Recall that the work in this thesis found limited effects of pulse duty on film composition. Within the literature, however, there is evidence to suggest that film composition is indeed affected by pulse duty [Landolt & Marlot 2003], [Liu & Pritzker 2003]. In both cases, the authors note that this occurs only at certain cycle lengths.

The first example is from the work of [Landolt & Marlot 2003] where the composition of Mo is measured in a Ni-Mo pulse-plated film. In their case, Mo is nobler than the Ni and is present at very low concentrations (like Cu in this thesis) so that deposition is diffusion-limited. At cycle lengths between 90 s and 1 s, pulse parameters do not play a significant role and Mo content is 10wt%.

Between 1 s and 1 ms however, the opposite is true. At about 60 ms, Mo content reaches 25wt% at 40% pulse duty and 17wt% at 60% pulse duty.

The second example is from the work of [Liu & Pritzker 2003] who consider a Pb-Sn fluoroborate electroplating solution. Here a very large range of cycle lengths is considered. In summary, it was found that the measured Pb content in PC electrodeposited films (with pulse duty = $t_{on}/(t_{on}+t_{off})$ = 80%) varies slightly, from 14wt% at ~80 ms cycle length to 18wt% at ~80 μs cycle length. However, the use of a cathodically-shifted waveform (pulse reversed; see Figure 3-7b in Chapter 3) caused the Pb content to vary widely from 2wt% at ~8 ms cycle length to 29wt% at ~60 μs cycle length. In the latter case, an electroplating current density is maintained for 80% of the cycle length, while an electroetching current density of the same magnitude is maintained for the remaining 20% of the cycle.

The example of [Liu & Pritzker 2003] is interesting in light of work by [Kim & Ritzdorf 2004] who consider the variation in Pb content of films that are PC plated using undisclosed bath chemistry. They vary the pulse duty while maintaining a constant 10ms cycle length. The authors observed about 48wt%Pb at 25% pulse duty and ~38%Pb at 100% pulse duty (DC plating). As stated in Chapter 4, the variance was attributed to changes in the pulsed diffusion layer, which would reflect differences in ion diffusivity to varying degrees. Note that the reduction potential for both ions is very similar.

Whisker Formation

As previously mentioned, a concern with Sn and Sn-Cu films is susceptibility to whiskering, though there is evidence supporting the use of Ni substrates (iNEMI, 2004-1) or engineered plating techniques [Bidin et al 2001], [Zhang & Abys, 2000], that claim to greatly reduce this problem. Further, [Nakamura et al 1994] explore the use of additives that affect the crystal orientation of Sn deposits from a 0.5 M H_2SO_4 solution. An earlier investigation by the same research group

[Keneko & Nezu 1989] reports the use of similar additives. Here, columnar Sn deposits are replaced by finer grains with better packing and a preferred (200) crystallographic orientation.

Such approaches may hold the key to reduced whiskering, due to lower compressive film stress. For example, [Bidin et al 2001] claim improvements in pure Sn deposits that exhibit larger-than-normal grain sizes and a whisker-inhibiting pyramidal-polygonal structure. Unfortunately, the authors do not expand upon the description, and no references are given to the literature. As a note of caution, [iNEMI 2004-2] states in their report that such claims from the literature have yet to be substantiated to their satisfaction.

Variable Pulse Waveforms

Recall that a number of processes can occur during plating off-time. These include recrystallization, adsorption of impurities and reduction of Cu^{2+} to Cu on the cathode surface [Puippe 1986-2]. An alternate form of the simple square wave is an anodically-shifted trace (as illustrated in Figure 3-7b of Chapter 3). In such a case there is no off-time. Rather, there is an extended period wherein a very small current flows in the opposite direction to plating: high-energy sites on the cathode are preferentially etched and the surface may be "cleaned" by desorption of impurities. It is not known whether this is a practical solution, however.

Extended Solderability work

After presenting the dip-and-look solderability work [Olsen, Ivey 2005], B. Christian from Research In Motion offered the use of a wetting balance tester for more in-depth study. The reported benefits of a wetting balance are quantitative measurement of wetting forces and accurate wetting times. Both sets of data are important for determining solderability.

In a private communication, B. Christian suggested the use of specially-prepared FR4 circuit boards from a company called PhotoCircuits. Use of the boards is important, since the pad shapes must be consistent. Literature from the British National Physics Lab website on solderability was also recommended.[1]

Final Comments

Summary

This work may be considered an introduction to electronic packaging techniques from a green perspective. As can be seen, the use of materials with lower impact on the environment and human health represents a challenge to the electronics industry. From a green perspective it is also necessary to use friendly process technologies, and this further complicates matters.

The usefulness of a sulphate electroplating system has been considered as a potential candidate for the challenge of Pb-free solderable finishes. To this end, the characteristics of plated and soldered films have been investigated. It was found that solderable finishes could be plated on Au and Cu substrates using an additive-free sulphate solution. Finally, such finishes showed enhanced solderability over bare Cu.

[1] A book entitled *Spreading and Wetting, 2) Solderability papers of the British National Physics Lab* website.